Conception des modulateurs sigma-delta d'ordre élévé pour des convertisseurs analogique-numérique en parallèle

Mohammad Javidan

ORSAY
N° d'ordre :

Université de Paris XI
Centre d'Orsay

École Supérieure d'Électricité
SUPÉLEC

THÈSE

présentée pour obtenir le grade de

DOCTEUR EN SCIENCES
DE L'UNIVERSITÉ DE PARIX XI ORSAY

Par

Mohammad JAVIDAN

CONCEPTION DES MODULATEURS SIGMA-DELTA D'ORDRE ÉLEVÉ POUR DES CONVERTISSEURS ANALOGIQUE-NUMÉRIQUE EN PARALLELE

Thèse soutenue le 18 décembre 2009

Commission d'examen :
MM.

Souhil MEGHERBI	Président
Dominique DALLET	Rapporteur
Maurits ORTMANNS	Rapporteur
Jean GODIN	Examinateur
Raymond QUERE	Examinateur
Philippe BENABES	Examinateur
Matthieu CHATRAS	Invité

Thèse préparée au Service des Mesures
École Supérieure d'Électricité

Design of high-order sigma-delta modulators for parallel analog-to-digital converters

Mohammad JAVIDAN

Department of Signals processing and Electronic Systems (SSE)

University of Paris XI, Centre d'Orsay

A thesis submitted for the degree of

PhilosophiæDoctor (PhD)

2009 December

1. President: Souhil Megherbi, professor (Dr.-Ing), Head of IUT Cachan-Paris XI university, Cachan, France. **Email**: souhil.meghrebi@u-psud.fr

2. Supervisor: Philippe Benabes, professor (Dr.-Ing), SSE department-Supelec, Gif sur yvette, France. **Email**: philippe.benabes@supelec.fr

3. Reviewer: Maurits Ortmanns, professor (Dr.-Ing), Institute Fur Mikroelektronik-Ulm university, Ulm, Germany. **Email**: maurits.ortmanns@uni-ulm.de

4. Reviewer: Dominique Dallet, professor (Dr.-Ing), IMS laboratory-Bordeaux university, Bordeaux, France. **Email**: dominique.dallet@ims-bordeaux.fr

5. Examiner: Jean Godin, Head of GCBH (Dr.-Ing), Alcatel-Thales III-V Laboratory, Route de Nozay, France. **Email**: jean.godin@3-5lab.fr

6. Examiner: Raymond Quere, professor (Dr.-Ing), C2S2 Laboratory-XLIM, Limoges, France. **Email**: raymond.quere@xlim.fr

7. Invited: Matthieu Chatras, professor, C2S2 Laboratory-XLIM, Limoges, France. **Email**: matthieu.chatras@xlim.fr

Day of the defense: 18 December 2009

Abstract

The present work is about design of convenient high-order continuous-time band-pass sigma-delta modulators for parallel A/D converters. First of all, an overview on the basic concepts of analog to digital conversion is presented.

The extended frequency band decomposition technique is chosen as a good solution for parallelism. The requirements of this technique are studied, including high resolution performance of the used converters at high frequencies.

A 6^{th}-order continuous-time band-pass single-stage sigma-delta modulator with a quantizer number of bits equal to 3 and an oversampling ratio equal to 64 is theoretically able to meet the objectives. However, a proper methodology of design is required in order to make a reliable design in practice since continuous-time modulators are sensitive to analog imperfections. This methodology must be able to overcome the practical issues such as the dependence of the modulator performance to the modulator central frequency as well as the issue of a robust stability margin.

For this aim, a new structure based on Weighted feedforward techniques providing an adequate control on the position of the poles of the noise-transfer-function by simple means is proposed. Moreover, the proposed structure provides a filtering-signal-transfer-function close to the modulator central frequency in order to increase the input dynamic range of the modulator.

An optimization method on the modifiable parameters of the proposed topology is developed in order to recover the performance of the modulator accounting analog imperfections. The system-level model of analog

components extracted from a transistor-level simulation must be used to guarantee the modulator performance in practice.

The methodology must be associated with a proper resonator capable of providing a large quality-factor at the required band of frequency. Of all the studied sorts of the resonators, Lamb-wave-resonators are chosen. Also solutions are considered in order to overcome the issues of this kind of resonators including the anti-resonance and low impedance connections.

Finally, a second-order sigma-delta modulator is chosen to benchmark the proposed solutions. AMS Bi-CMOS 0.35 μm technology kit is used and the modulator is designed and simulated in layout-level. The results approve the efficiency of the proposed solutions.

To my parents...

Acknowledgements

I would like to take this opportunity to acknowledge all those who gave me the possibility to complete this thesis and who have made the last three years of my life a memorable and unforgettable experience.

I am deeply indebted to my supervisor Prof. Philippe Benabes. Thanks for your support, for your intelligent guidance, for your valuable comments when I needed them must. A few words can not certainly express the extent to which I am indebted to your positive influence.

I have furthermore to thank the head of the department Prof. Gill Fleury, who supports me kindly during my thesis and encouraged me to go ahead with my thesis.

I have to thanks Prof. Jerome Juillard, for his stimulating support interest and valuable hints.

I have to thanks Prof. Matthieu Chatras, from XLIM laboratory, for his Collaboration and constructive comments during the analysis of the lamb-wave-resonators

I have to thanks Mr. Francis Trelin, for assistance during the process of laying out my chips.

I have to thanks Prof. Richard Kielbasa and Prof. Morgan Roger for all their help.

I have to thanks my colleagues supported me in my research work. I want to thank them for all their help, support, interest and motivation. Especially I am obliged to Mr. Luc Batalie, Ms. Karine Bernard, Mr. Bahman Soheilian and Mr. Zhiguo Song.

Finally, my most grateful thanks are reserved for my parents for their encouragement, patient, support and love, and for believing in me and having made all of this possible.

Glossary

ADC	Analog to Digital Converter
BAW	Bulk Acoustic Wave
Bi-CMOS	Bipolar and CMO
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
CTOC	Current TO Current converter
CTOV	Current TO Current converter
DAC	Digital to Analog Converter
DR	Dynamic Range
DSP	Digital Signal Processors
DT	Discrete Time
EFBD	Extended Frequency Band Decomposition
ENOB	Effective number of bits
ERWB	Effective Resolution BandWidth
FBD	Frequency Band Decomposition
Gm-C	Classical resonator based on trans-inductance amplifier and integrated capacitance
Gm-LC	Classical resonator based on integrated capacitance and inductance
HZ	Half delay Zero
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LSB	Least Significant Bit
MASH	Multi Stage noise SHaping
MSCL	Multi Stage Closed Loop
NRZ	Non Return to Zero
NTF	Noise Transfer Function
OSR	Over Sampling Ratio
RF	Radio Frequency

RZ	Return to Zero
SAW	Surface Acoustic Wave
SMASH	Sturdy Multi Stage noise SHaping
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
STF	Signal Transfer Function
TI$\Sigma\Delta$	Time Interleaved Sigma-Delta
VTOC	Voltage TO Current converter
WiFi	Wireless Fidelity
$\Sigma\Delta$	Sigma-Delta
$\prod \Sigma\Delta$	Parallel Sigma-Delta

Contents

List of Figures

LIST OF FIGURES

List of Tables

1

Outline

1.1 Motivations

The new generations of mobile systems are not anymore a simple communication system limited to transmission of the human voice. Nowadays, the trend is to design multi-standard telecommunication systems able to process different standards. The integration of various applications (like GPS, TV, Bluetooth, etc) in mobile systems imposes new requirements including a larger frequency bandwidth to satisfy high data-rate transfer, and low power consumption for a longer autonomy. Thus highly-integrated, high-resolution and multi-standard systems are required [1].

The software radio solution was presented, for the first time, by J. Mitola [2], [3] to answer the new requirements of telecommunication markets. The concept of a software radio receiver is presented in figure 1.1. The idea is to replace the analog components by software to achieve a flexibility of reconfiguration without the need for material modification. For this aim, the Analog to Digital Converter (ADC) must be brought as close as possible to the antenna.

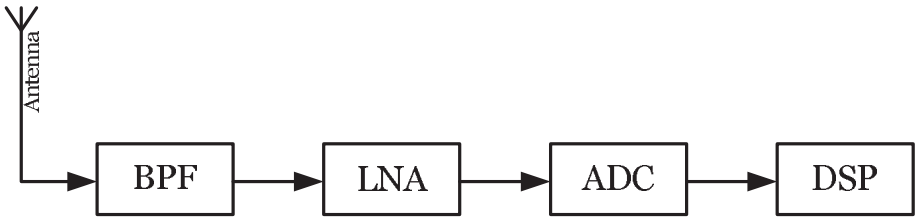

Figure 1.1: The principle of software radio solution.

1. OUTLINE

Several issues must be overcome [4], [5]. Application Specific Integrated Circuits (ASICs) must be replaced by software implementation in DSPs. The system must support a large input dynamic range as there is no specification for applications. The main issue concerns the ADC functionality. A large band A/D converter to cover the frequency band of the integrated standards is required.

Parallelism is a solution to increase the ADC bandwidth without degrading its performance. The idea consists in putting ADCs in parallel where each of them process a portion of time or frequency of the input signal. In this context, because of wireless multi-function constraints, the employed converter must be able to work at high frequencies with high resolution. Moreover, the power consumption and the required chip area must be as small as possible.

Nyquist-rate ADCs are not able to meet the requirements of parallel structures. Pipeline ADCs [6], [7] and Approximations successive ADCs [8], [9] do not satisfy the demands in terms of speed. Flash ADCs [10], [11], are able to work at the required frequency but they have two major disadvantages in terms of chip area and power consumption. For an n-bits resolution Flash ADC, $2^n - 1$ comparators are needed. As a result, high resolution Flash ADCs are big circuits with large power consumption because of the employed number of comparators. The number of comparators can be reduced by folding techniques [12], [13]. Indeed, during a ramp input signal, folding ADCs re-use the comparators multiple times. Although for a m-times n-bits resolution folding A/D the required number of comparators can be reduced from $2^n - 1$ to $\frac{2^n}{m}$, they are still low-pass converters.

Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulator ADCs are good candidates to be employed in parallel systems. High-order $\Sigma\Delta$ modulators are high resolution converters capable of working at high frequencies. Based on $\Sigma\Delta$ modulators, various methods are proposed to implement a parallel ADC. Time Interleaved Sigma-Delta (TI$\Sigma\Delta$) [14], Parallel Sigma-Delta ($\Pi\Sigma\Delta$) [15], Frequency Band Decomposition (FBD) [16], [17] and Extended Frequency Band Decomposition (EFBD) [18] are the most well-known ones. A comparative study on the presented methods is done in [19].

The TI $\Sigma\Delta$ solution has the lowest hardware complexity, but it has two main drawbacks. First, the whole frequency band between 0 Hz and the sampling frequency (f_s) is converted while the wanted signal band is generally a portion of the whole

frequency band. Moreover, the TI solution is highly sensitive to both offset and gain mismatches of analog parameters resulting in distortion and unwanted tones.

The FBD is another solution to widen the converter bandwidth by using N parallel band-pass modulators, where each modulator processes a portion of the frequency band of interest. Although analog mismatches may result in distortion of the FBD Signal Transfer Function (STF), they have no non-linear effects.

The EFBD is an improved system, compared with the FBD, based on the same principle. Two extra converters are employed to reduce the sensitivity of its STF to analog imperfections. This solution is vastly studied in [20].

Regardless of the chosen solution of parallelism, the used structure of $\Sigma\Delta$ modulator must be able to provide the given resolution at high frequencies. Although high-order CT $\Sigma\Delta$ modulators are mandatory to this end, they suffer seriously from instability issues and sensitivity to analog imperfections. A new methodology of design of high-order CT $\Sigma\Delta$ modulators, compatible with the parallel context, is then required.

1.2 Objectives and completed work

The design of an A/D converter able to provide a bit resolution equal to 16-bits across a frequency band between $0.2f_s$ and $0.3f_s$ accounting practical issues like analog imperfections is the main objective of the present work. Extracting the requirements of EFBD systems results in choosing 6^{th}-order CT single-stage modulators. However in order to satisfy the requirements, two kinds of problems must be overcome which are the sensitivity of CT modulators to analog imperfections as well as the need of a resonator able to perform a high Q-factor.

To overcome the first problem, a new structure of 6^{th}-order modulators based on weighted feedforward techniques is used. The main advantage is the possibility of establishing a robust stability regime by optimizing the value of few coefficients. Analog imperfections are also considered in the developed optimization method. On the other side the need of a high Q-factor leads us to use piezo-electric resonators. We will show that Lamb wave resonators are theoretically more interesting than other kinds of piezo-electric resonators. Finally the design of a second-order modulator is done to verify the reliability of the proposed solutions.

1.3 Organization of the statement

In the **chapter II**, the basic concepts and the principle of the operation of $\Sigma\Delta$ modulators are explained as well as different classes of them. The linear model of the quantizer allowing to apply linear analysis method on $\Sigma\Delta$ modulators and various criterion to describe the performance of a modulator are also presented.

In the **chapter III**, the requirements of an EFBD system are studied and the characteristics of a proper modulator to attain the requirements are extracted. Afterward, the difficulties to implement the extracted characteristics are explained.

In the **chapter IV**, various sorts of resonators are studied in order to chose the most compatible with requirements. Lamb wave resonators being theoretically the most convenient have also some disadvantages. The relative advantage and disadvantages of them are studied and some solutions to overcome the major issues are then proposed.

In the **chapter V**, the major issues of high-order CT $\Sigma\Delta$ modulators are studied. It is shown that a new methodology of design is required in order to establish a robust stability regime while maintaining the resolution. To this end, a new structure of 6^{th}-order modulators based on weighted feedforward techniques is proposed. Although a simple synthesis of an equivalent DT modulator with the proposed structure does not satisfy the demands, it is possible to attain the objectives relying on the flexibility of this structure. Then an optimization method on the modifiable parameters of this structure is developed. In order to be reliable in practice, analog imperfections are considered in system-level.

In the **chapter VI**, the design of a second-order modulator in layout-level with AMS Bi-CMOS $0.35\mu m$ technology is explained. Although the theoretical work of the present work is focused on the design of 6^{th}-order modulators, the design of a second-order modulator is considered because of missing informations about practical behavior of Lamb wave resonators. Indeed, this design is done for the aim of testing the compatibility of Lamb wave resonators with the loop of $\Sigma\Delta$ modulators.

The **conclusion** makes an overall review on the done works as well as presenting the perspectives to improve and accomplish the studied targets.

2

Introduction

2.1 Basic concepts

2.1.1 Analog-to-digital conversion

Analog-to-digital conversion is a process to convert a continuous-time signal ($x(t)$) into a multi-level or digital signal ($y(n)$) as it is shown in figure 2.1.

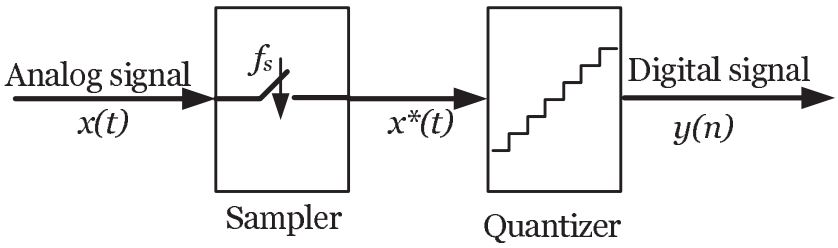

Figure 2.1: Analog-to-digital conversion.

The time index n of a digital signal ($y(n)$) is an integer number. The sampler output is a Discrete-Time (DT) signal presented by $x^*(t)$ where t is equal to nT_s and T_s is the sampling period equal to $\frac{1}{f_s}$ where f_s is the sampling frequency. The relation between $x(t)$ and $x^*(t)$ is as follows:

$$x^*(t) = \sum_{n=0}^{\infty} x(t)\delta(t - nT_s), \tag{2.1}$$

where $\delta(t)$ is:

$$\begin{cases} 1, & t = 0 \\ 0, & \text{elsewhere} . \end{cases} \tag{2.2}$$

An ADC transforms first the CT input signal ($x(t)$) into a DT signal ($x^*(t)$). Afterward, each sample is approximated by a quantizer to transform $x^*(t)$ into a digital signal ($y(n)$) containing a sequence of finite precision or quantized samples.

2.1.2 Quantization error

The quantizer rounds the input signal ($x^*(t)$) to the nearest level, as illustrated in figure 2.2.

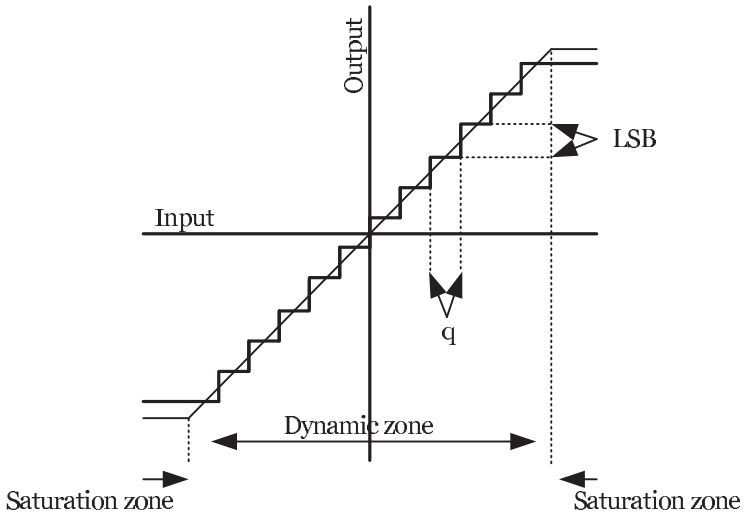

Figure 2.2: Quantization principle.

Quantization introduces an error signal that depends on how the signal is being approximated. This error, called the quantization error ($e(n)$), is on the order of one Least-Significant-Bit (LSB) in amplitude [21]. The quantization error is in general small compared with a full amplitude input signal range but it becomes relatively larger when the input signal gets smaller. The relation between $e(n)$, $x^*(t)$ and $y(n)$ is given by:

$$e(n) = y(n) - x^*(t). \tag{2.3}$$

Although the quantizer is a non-linear system and $e(n)$ is an unknown function, various approximate linear models of the quantizer are proposed to recognize $e(n)$ and

to be able to apply the classical methods of analysis to systems containing a quantizer. These models are all based on the asymptotic results of Bennet [22] or the exact results of Widrow [23] and Sripad [24] .

2.1.2.1 Model of Bennet

Bennet describes the conditions under which the quantization error can be modeled by white noise. Assuming a B-bits quantizer, the number of available levels to quantize $x^*(t)$ is equal to 2^B. Thus, the interval between successive levels (q) is given by:

$$q = \frac{1}{2^B - 1}. \tag{2.4}$$

In [22], it is shown that for the following conditions :

1. The input signal does not exceed the dynamic zone of the quantizer.
2. The quantizer number of bits (B) is sufficiently large.
3. The amplitude of the input signal is large compared with LSB.

$e(n)$ is a random quantity in each quantization step with equal probability and the variance of $e(n)$, the noise power (σ_e^2), can be calculated as follows [25]:

$$\sigma_e^2 = \frac{1}{q}\int_{-q/2}^{q/2} e^2 \, \mathrm{d}e = \frac{q^2}{12} = \frac{2^{-2B}}{3}. \tag{2.5}$$

As a result, the quantizer can be replaced by its linear model presented in figure 2.3.

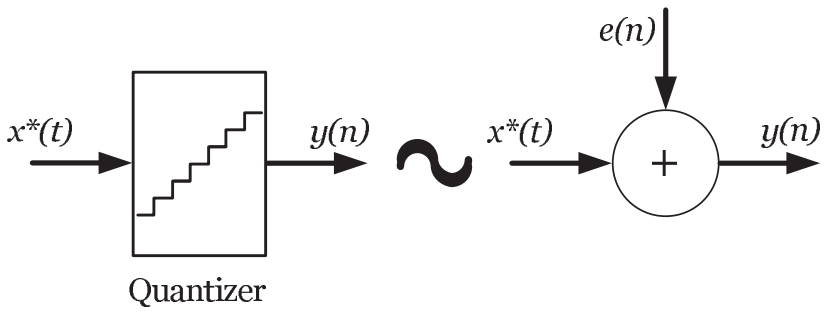

Figure 2.3: Quantizer linear model.

In analog-to-digital conversion since the noise power is spread over the entire frequency range equally, the level of the noise power spectral density can be expressed as follows:

$$N(f) = \frac{q^2}{12 f_s} = \frac{2^{-2B}}{3 f_s}. \tag{2.6}$$

The noise level is a function of the quantizer number of bits and the sampling frequency. It becomes smaller when f_s or B get larger. Figure 2.4 shows the spectrum of the quantization noise in the signal frequency band $[-f_b, f_b]$.

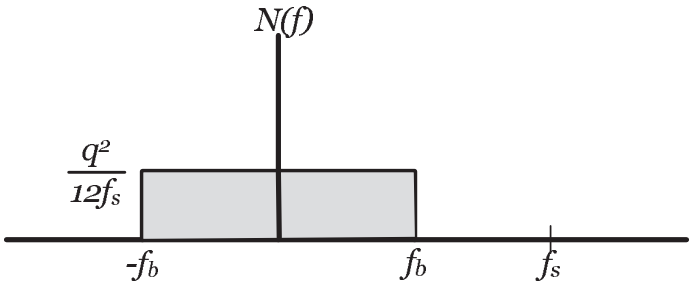

Figure 2.4: Noise spectrum of the quantization error.

2.1.2.2 Low-order quantizer

The linear model of the quantizer is indispensable to analyze ΣΔ modulators [26]. The Noise Transfer Function (NTF) and the STF of ΣΔ modulators are found through this model. Although the model of Bennet is valid in a high-order ΣΔ modulator loop regardless of the quantizer number of bits, for low-order modulators this model is reliable when the quantizer number of bits is sufficiently large. The quantization noise of a low-order (second or fourth) modulator containing a low-order quantizer ($B = 1$ or 2), does not have an equal probability for each quantization step [27], [28], [29]. It should be noted that in a ΣΔ modulator loop, the quantizer number of bits is in general small because of practical considerations including chip area and power consumption.

The linear model may be modified, as it is shown in figure 2.5, to improve the approximation of low-order quantizers. The quantizer is modeled by a gain stage (η) associated with an additive white noise [30], [31], [32], [33], [34].

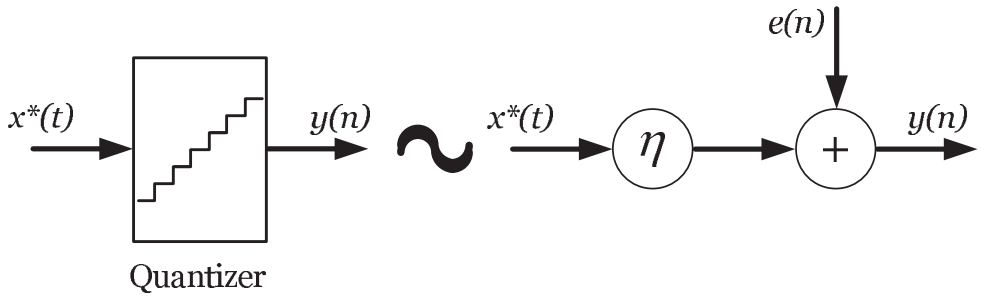

Figure 2.5: The linear model of a low-order quantizer.

Although η is almost equal to one for high-order quantizers, for low-order ones its value depends on the modulator structure and on the amplitude of the input signal. Therefore, it is a variable number which is difficult to be estimated. In order to release the analysis of the modulator from η, one may use a dither signal [35] which adds to the system an uncorrelated noise to minimize the correlation between the input signal and the quantization error. The dither must be small enough to not deteriorate the modulator performance and large enough to result in a whit noise. Other models of low-order quantizers are also proposed in [36], [37].

2.1.3 Oversampling and decimation

Regarding the sampling frequency, the ADCs may be categorized into Nyquist-rate ones and oversampling ones. The quantization process is different from one to another. Nyquist-rate ADCs sample the input signal with the minimum sampling rate required to avoid aliasing while oversampling ADCs use a sampling rate significantly larger than the Nyquist-rate. Afterward, a digital decimation filter is employed to reduce the signal rate to the Nyquist-rate.

Regardless of the quantization process, oversampling eases the design of the anti-aliasing filter. Assuming a typical signal with a bandwidth equal to f_b, figure 2.6.a compares the anti-aliasing filter required for a Nyquist-rate sampled signal ($f_s = 2f_b$) and a two-times oversampled signal ($f_s = 4f_b$).

The anti-aliasing filter of Nyquist-rate ADCs requires a flat response with no phase distortion over the frequency band of interest. Moreover, in order to prevent signal distortion because of aliasing, all signals above f_b must be attenuated, for example, by at least 96-dB to achieve 16-bits of dynamic resolution. It should be noted that these

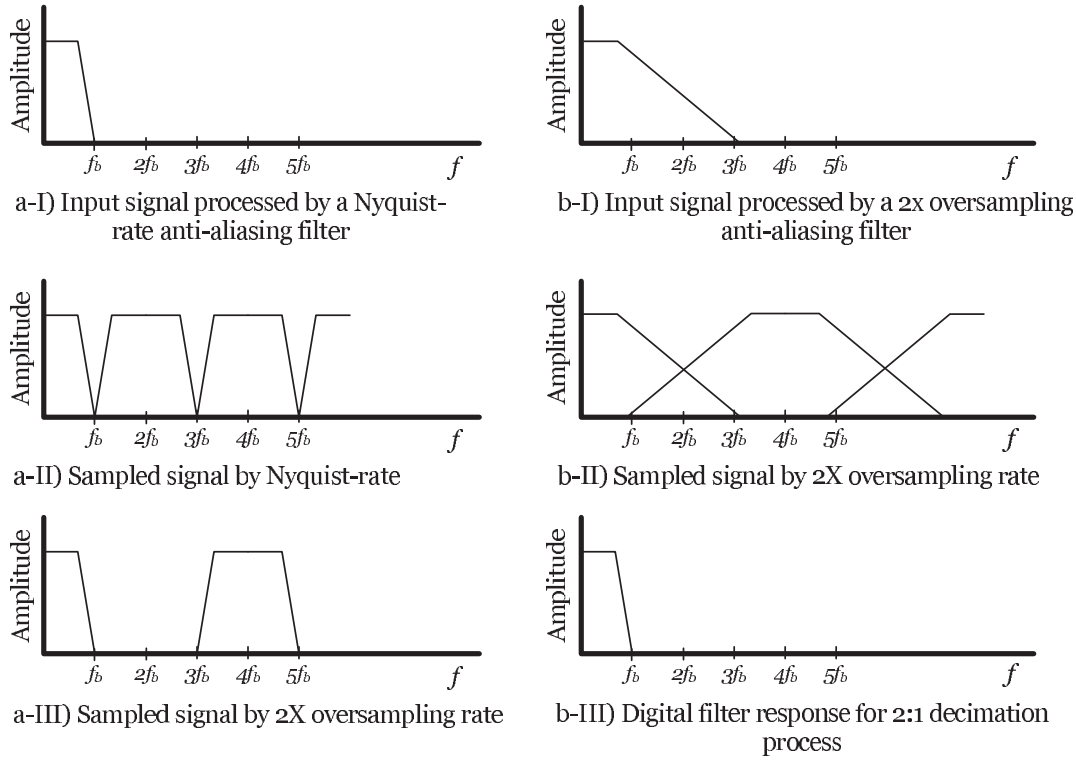

Figure 2.6: Comparison the Nyquist-rate anti-aliasing filter with two-times oversampling anti-aliasing filter (a), the quantization process of a 2x oversampling ADC(b).

requirements are tough to meet with an analog low-pass filter. Considering the same signal sampled at $4f_b$, the anti-aliasing filter must only present a flat performance up to f_b and eliminate signals above $3f_b$ (figure 2.6.a). Clearly, the design of an oversampled anti-aliasing filter is much easier than a Nyquist-rate one. However, since the sampling rate is equal $4f_b$, a sample rate reduction filter is required but it is implemented in digital domain as opposed to anti-aliasing filters which are implemented with analog circuitry.

The two-times oversampling can be extended to N-times oversampling converters. Considering a full precision quantizer, the total noise power of oversampling converters and Nyquist-rate ones are the same and they are given by equation 2.5. However, the difference is in the power of the residual noise in the bandwidth of interest. The residual noise power is given by:

$$N_b = \int_{-f_b}^{f_b} N(f)\, df = \frac{2 f_b q^2}{12 f_s}. \tag{2.7}$$

The in-band noise of an oversampling converter is much smaller than the in-band noise of Nyquist-rate converters when f_s is much larger than f_b. Reducing the in-band noise is completed by using a decimation filter to provide increased resolution. Figure 2.7 compares the level of the in-band noise of a Nyquist-rate ADC with a two-times and a three-times oversampling ADCs.

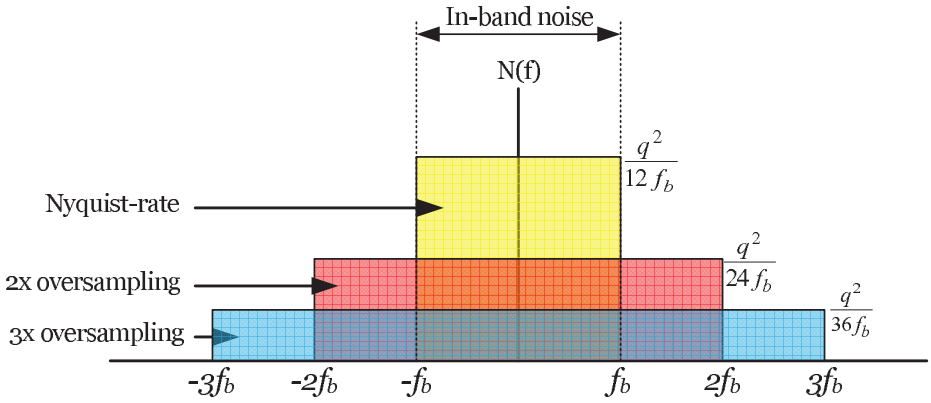

Figure 2.7: Comparison the in-band noise of Nyquist-rate ADCs and that of oversampling ADCs.

2.1.4 Noise shaping

Although the oversampling process increases the ADC resolution, the main disadvantage is the linear relation between the noise level and $\frac{1}{f_s}$. Considering the technology limits, it is not possible to increase arbitrarily the sampling frequency. Therefore, the resolution of oversampling ADCs is limited by technology. In order to improve the resolution, oversampling ADCs must be associated with a noise shaping system. The idea consists in rejecting the quantization noise from the frequency band of interest to out-of-band frequencies.

2.1.4.1 Delta conversion

Using feedbacks to reject the in-band noise has been introduced in Delta modulation for the first time [38]. Delta modulation is based on quantizing the change in the signal

from sample to sample rather than the absolute value of the signal at each sample. The error term $(x(t) - \widehat{x}(t))$, in each sample, is quantized and used to make the next error term (figure 2.8).

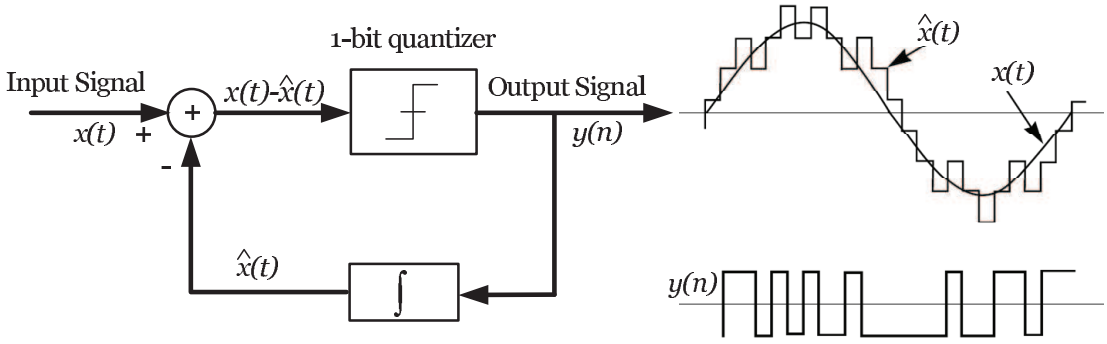

Figure 2.8: Delta modulation principle.

The error signal is smoothed by a low-pass filter. As a result, for a high frequency input signal or a high speed rise of the input signal, the modulator is overloaded. Then, the performance of Delta modulation is limited in terms of speed.

2.1.4.2 Sigma-delta conversion

The arrangement shown in figure 2.9 is called a ΣΔ modulator [39]. The name ΣΔ

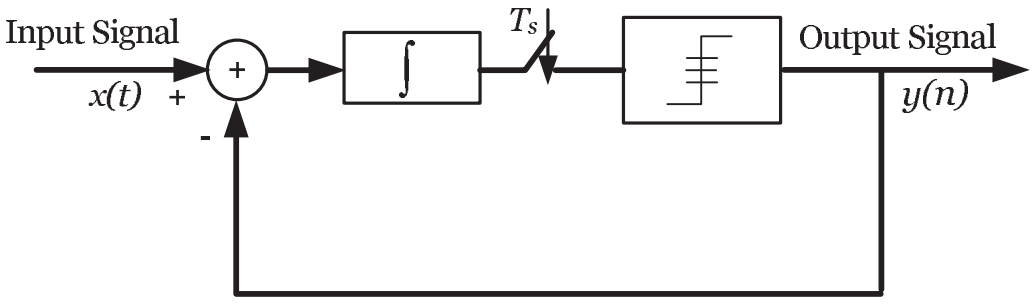

Figure 2.9: ΣΔ modulation.

modulator comes from putting the integrator (Σ) in front of the delta modulator. ΣΔ modulation is based on two beneficent function being the oversampling and the noise shaping [40], [41], [42], [43].

A first-order low-pass DT ΣΔ modulator is chosen for explaining the noise shaping principle. Note that the modulator order corresponds to the number of employed integrators in low-pass context and two-times of the number of employed resonators in band-pass context. Figure 2.10 shows the linear model of the first-order low-pass modulator.

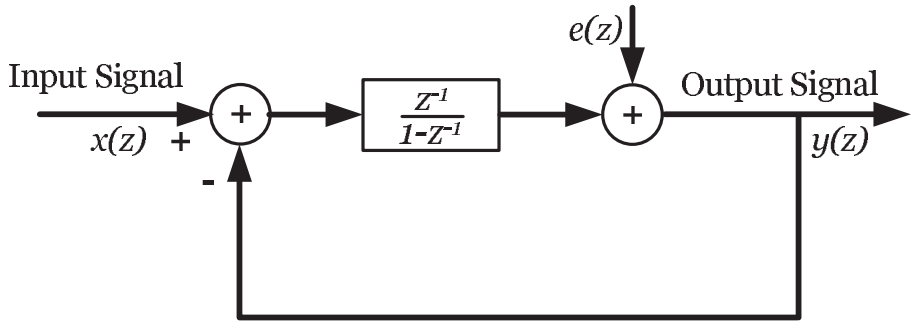

Figure 2.10: Linear model of a first-order low-pass DT ΣΔ modulator.

The system equation (the relation between $y(z)$, $x(z)$ and $e(z)$) is:

$$y(z) = (x(z) - y(z))\frac{z^{-1}}{1 - z^{-1}} + e(z). \tag{2.8}$$

This results to calculate the STF and the NTF as follows:

$$\begin{cases} \text{STF} = \frac{y(z)}{x(z)} = z^{-1}, \\ \\ \text{NTF} = \frac{y(z)}{e(z)} = \frac{1-z^{-1}}{z^{-1}}. \end{cases} \tag{2.9}$$

Since the STF is a delay function, the input signal is left unchanged as long as its frequency content does not exceed the filter cut-off frequency. On the other side, the NTF is a high-pass filter and rejects the noise into a higher frequency band. A ΣΔ modulator generates an output which can be averaged over several input sample periods to produce a very precise result. The averaging is performed by decimation filters following the modulator. The noise spectrum of a Nyquist-rate ADC, an oversampling ADC and a first-order low-pass ΣΔ modulator are compared in figure 2.11.

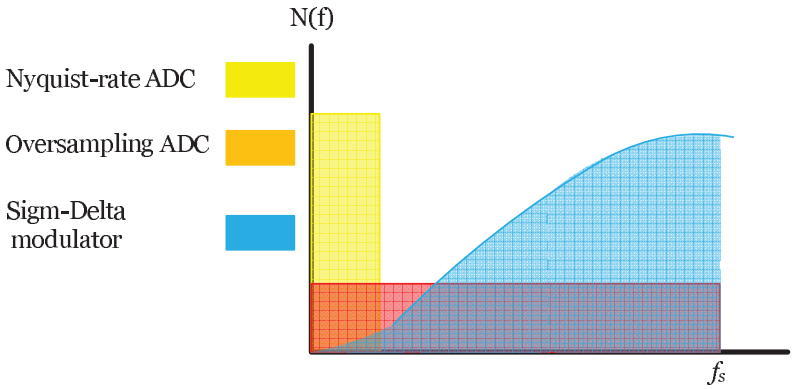

Figure 2.11: Comparison the noise spectrum of a Nyquist-rate ADC, an oversampling ADC and a first-order low-pass ΣΔ modulator.

2.1.5 From low-pass to band-pass conversion

Converting a high frequency signal requires a corresponding band-pass modulator. Indeed, the modulator central frequency (at which the in-band noise is minimal) must match the input signal frequency. Figure 2.12 compares the structure of a low-pass and a band-pass ΣΔ modulator. In DT domain, a band-pass modulator is obtained

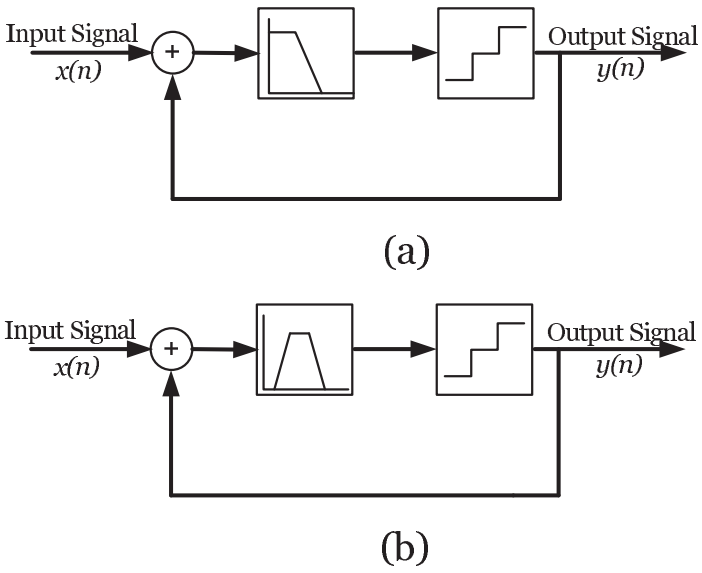

Figure 2.12: Low-pass modulator (a) and band-pass modulator (b) in DT domain.

from a low-pass one by replacing the integrators with resonators. Shifting the low-pass

modulator to the desired frequency can be done by the transfer given by [44], [46]:

$$z^{-1} \quad \Longleftrightarrow \quad z^{-1}\frac{z^{-1}-\frac{p}{2}}{1-\frac{p}{2}z^{-1}}, \tag{2.10}$$

where p determines the desired central frequency (f_c) and is given by:

$$p = 2\cos\left(2\pi\frac{f_c}{f_s}\right). \tag{2.11}$$

The resonator obtained from an integrator through equation 2.10 is given by:

$$\frac{z^{-1}}{1-z^{-1}} \quad \Longleftrightarrow \quad \frac{\frac{p}{2}z^{-1}-z^{-2}}{1-pz^{-1}+z^{-2}}. \tag{2.12}$$

The properties of the low-pass modulator in terms of stability and resolution are conserved after the transfer.

2.2 Band-pass continuous-time sigma-delta modulator

2.2.1 Discrete-time or continuous time

The structure of a CT ΣΔ modulator is compared with that of a DT modulator in figure 2.13. The input signal of DT modulators is in discrete-time domain (already

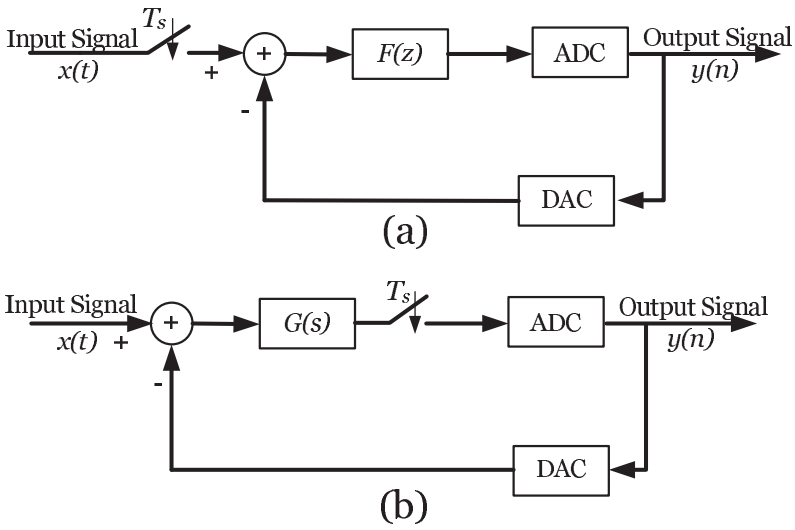

Figure 2.13: DT ΣΔ modulator structure (a), CT ΣΔ modulator structure (b).

sampled). Therefore, the modulator filters are also implemented in DT domain. On

the contrary, sampling is done before the quantizer in CT modulators and the modulator filters are implemented in CT domain. DT filters are generally designed by switched capacitor techniques. Although switched capacitor techniques are advantageous in terms of flexibility of design and precision, their speed cannot exceed from tens of MHz because of the limited bandwidth of the required operational amplifiers [47]. In addition, the speed of the charge transmission of the commutators is also limited. Another disadvantage which results in limiting the speed of DT modulators, is the sampling noise which is combined with the input signal while in CT modulators the sampling noise becomes a part of the quantization noise and is rejected into out-of-band frequencies by the NTF [48].

CT modulators are able to perform at high frequencies because of CT filter techniques [49]. It is generally feasible to clock CT $\Sigma\Delta$ modulators at much higher frequencies than DT $\Sigma\Delta$ modulators. Additionally, sampling in the modulator loop results in diminishing the thermal noise in the modulator frequency band [50]. Furthermore, CT analog circuits are less demanding than their DT counterparts in terms of power consumption. However, they are not an ideal solution. The design of Digital to Analog Converter (DAC) in the feedback path of CT modulators is difficult because of the sensitivity of the modulator performance to the DAC functionality. Compared with DT modulators, CT modulators are sensitive to clock jitter defined as the time variation or the peak-to-peak displacement (Δt) of the clock signal [51]. The feedback signal of DT modulators has an exponential form and the charge transmission is almost completed at the clock rise-time (figure 2.14.a). On the contrary, DAC output of CT modulators is a rectangular signal (figure 2.14.b). Therefore, clock jitter results in losing an important quantity of charge.

In addition, CT modulators are sensitive to the loop delay. This delay is the sum of the delays produced by all the analog and digital components of the modulator loop. In chapter IV, it is shown that modifying the loop delay changes the NTF poles position. A non-optimized loop delay may bring the NTF poles out of the unit circle and make the system unstable. Nevertheless, the increasing demand for high-speed high-resolution and low-consumption analog-to-digital conversion can be satisfied only by using CT $\Sigma\Delta$ modulators.

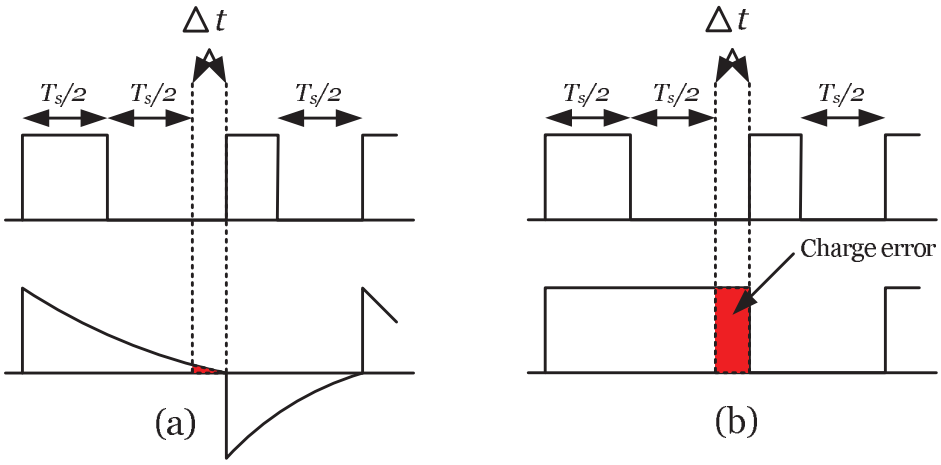

Figure 2.14: Influence of clock jitter on charge loss in DT (a) and CT (b) modulators.

2.2.2 From discrete-time to continuous-time

There exist various methods and toolboxes to find the global filter of a DT modulator corresponding to demands. Indeed, the design of DT modulators has progressed and the design of CT modulators may lean to this progress through the synthesis of CT modulators from their DT counterparts. However, the problem is not a simple transform from z domain ($F(z)$) to s domain ($G(s)$). The modulators in figure 2.13 are equivalent if they produce the same output for the same input at each sampling period.

As a result, the functionality of the ADC and the DAC should be taken into account in the transformation in order to ensure the equivalence between DT and CT circuits. The parameters to be considered include the internal delays and the non-linearity of the ADC and the DAC as well as the rise time and the form of the ADC+DAC output [52], [53]. An approach with these objectives is presented in [54]. The delays introduced by both the DAC and the ADC and the shape of the DAC output signal are taken into account. Standard tools available in symbolic calculation softwares, such as Laplace and z-transforms, are employed. This approach is put in equation as follows:

$$F(z) = (1 - z^{-1}) Z_T\{L^{-1}[G(s)B(s)]\} + \underbrace{\sum\nolimits_k a_k z^{-k}}_{D(z)}, \tag{2.13}$$

where L^{-1} denotes the inverse Laplace transform, Z_T is the z-transform at the sampling period (T_s) and $B(s)$ denotes the delay and the non-ideality parts of DAC and ADC

functionalities. The response of the DAC and the ADC, considered as a single block, is modeled by figure 2.15.

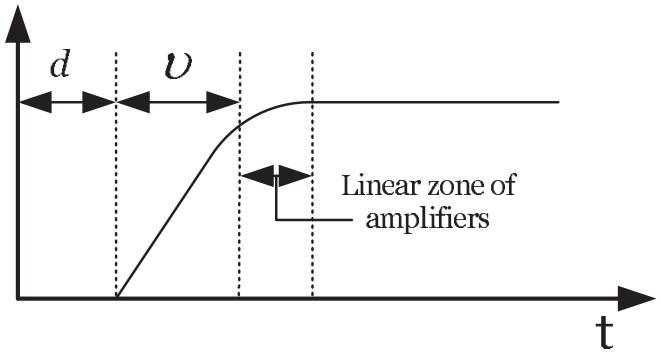

Figure 2.15: Model of the response of the ADC+DAC.

In this model, the speed of the ADC+DAC is described by the rise time (ν) and the loop delay is described by d. For the sake of the simplicity, the linear zone of the employed amplifier resulting in a non-linear zone of the ADC+DAC response is neglected. Then $B(s)$ is given by:

$$B(s) = \frac{e^{-ds} - e^{-(d+\nu)s}}{\nu s}. \tag{2.14}$$

$D(z)$ is added for ensuring an exact solution of equation 2.13. Indeed, without $D(z)$, it is possible that when $d \neq 0$ or $\nu \neq 0$, equation 2.13 has no exact solution. Implementing $D(z)$ demands some system modifications. Figure 2.16 shows a possible implementation when the ADC delay is sufficiently small.

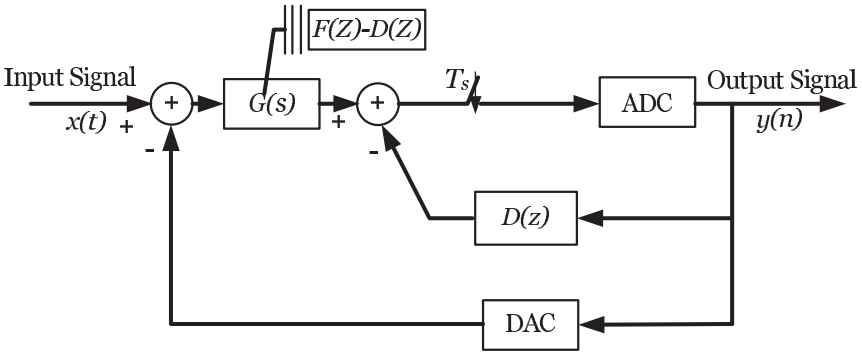

Figure 2.16: A possible implementation of equation 2.13.

When the internal delay of the ADC is larger than $1T_s$ (which is usually the case), not all the terms of $D(z)$, especially the low-order terms, can be implemented through the ADC output. Therefore, the topology of figure 2.16 is useless in practice. New implementation methods are required when the ADC delay is large. In [54] an alternative topology is proposed. This topology is shown in figure 2.17.

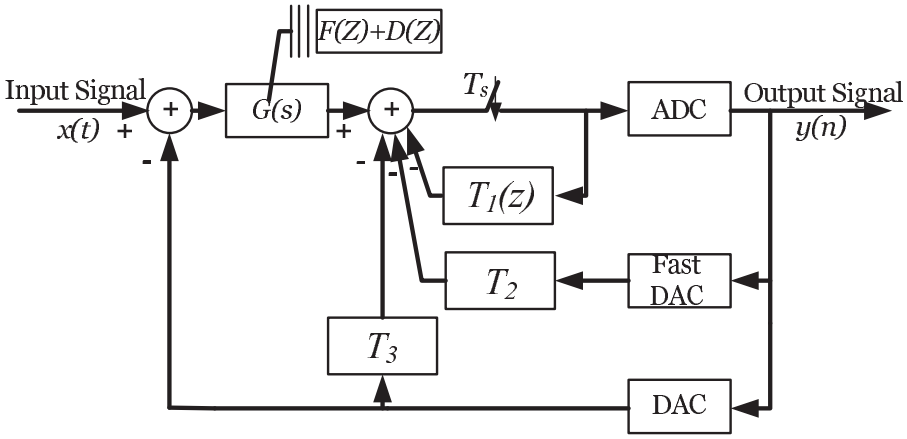

Figure 2.17: Proposed topology in [54] for implementing $D(z)$.

As it is shown, the terms of $D(z)$ are implemented in three ways:

1. $T_1(z)$: The first terms of $D(z)$, corresponding to a delay value less than the ADC delay, are implemented through the sampler output to avoid the ADC delay.

2. T_2: The intermediate terms of $D(z)$, corresponding to a delay value larger than the ADC delay but less than the loop delay (ADC+DAC delay), may be implemented by a fast DAC through the ADC output.

3. T_3: The last term of $D(z)$, corresponding to a delay larger than the loop delay, can be implemented from the DAC output.

2.3 Global loop filter structures

There exist various structures to synthesize the global filter transfer function ($G(s)$) of the modulator [21]. One may classify them in two general types including single-stage structures and multi-stage ones. Multi-stage topologies are sensitive to the inter-stage

coefficients error. Therefore, their performance is disappointing in the CT domain but the advantage is the stability of high-order modulators because they are based on cascading low-order modulators [46], [55]. On the other side, single-stage modulators are quite immune to the coefficient errors compared with multi-stage modulators. The main obstacle to overcome is the stability of high-order single-stage modulators.

2.3.1 Multi-stage modulators

In order to synthesize a $(2n)^{th}$-order band-pass modulator, n low-order (second-order or fourth-order) band-pass modulators are put in cascade. They are classified in different types [44].

2.3.1.1 MASH structures

Assuming that $H_1(z)$ and $H_2(z)$ are the transfer functions of second-order $\Sigma\Delta$ modulators, figure 2.18 explicits the topology of a fourth-order MASH $\Sigma\Delta$ modulator. The structure is presented in DT domain for the sake of understanding the principle.

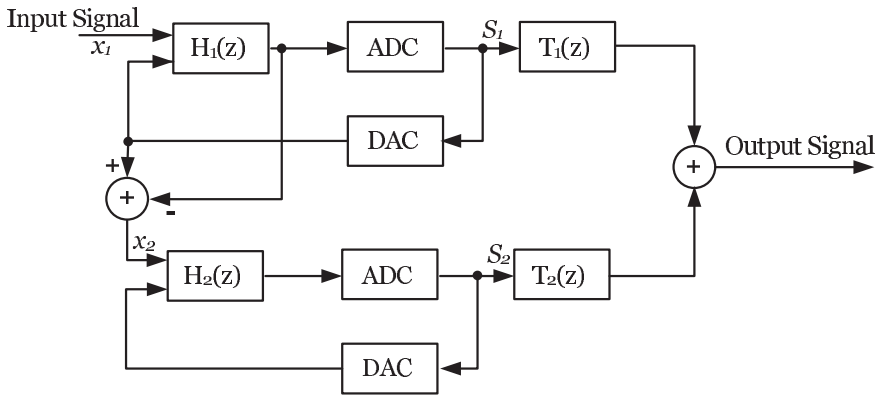

Figure 2.18: Fourth-order MASH topology.

The input of each stage is the quantization noise of the previous stage except for the first modulator [56], [57] and the output signal (S_i) of each stage is given by:

$$\begin{cases} S_1(z) = \mathrm{STF}_1(z)x_1(z) + \mathrm{NTF}_1(z)e_1(z), \\ S_2(z) = \mathrm{STF}_2(z)e_1(z) + \mathrm{NTF}_2(z)e_2(z). \end{cases} \tag{2.15}$$

where e_1 and e_2 are respectively the produced noise by the first and the second stage. $T_1(z)$ and $T_2(z)$ are calculated by:

$$T_1(z)\mathrm{NTF}_1(z) - T_2(z)\mathrm{STF}_2(z) = 0, \tag{2.16}$$

to eliminate $e_1(z)$ from the output signal. One solution consists in choosing $T_1(z)$ equal to $\mathrm{STF}_2(z)$ and $T_2(z)$ equal to $\mathrm{NTF}_1(z)$:

$$\begin{cases} T_1(z) = \frac{H_2(z)}{H_2(z)+1}, \\ T_2(z) = \frac{1}{H_1(z)+1}. \end{cases} \tag{2.17}$$

Replacing $H_i(z)$ by a second-order low-pass $\Sigma\Delta$ modulator results in achieving the same output signal (S) as a fourth-order low-pass $\Sigma\Delta$ modulator (equation 2.18) while the stability criterion of the resulted modulator is the same as a second-order modulator.

$$S(z) = T_1(z)S_1(z) - T_2(z)S_2(z) = Z^{-4}x_1(z) - (1-z^{-1})^4 b_2(z). \tag{2.18}$$

Perceptibly, the output signal is sensitive to the precision of $T_1(z)$ and $T_2(z)$. This is the main reason for which MASH topologies are not suitable for CT applications. The functionality of $T_1(z)$ and $T_2(z)$ is deteriorated, in the CT domain, because of analog imperfections.

2.3.1.2 MSCL structures

MSCL structures put low-order modulators (second-order or fourth-order) in cascade like MASH structures to achieve a high-order modulator [58]. The difference is replacing $T_1(z)$ and $T_2(z)$ by an extra feedback between the structure output and the input (figure 2.19).

Similar to MASH structures, the second stage processes the produced quantization noise by the first stage. An exact calibration of the feedback path is needed for adjusting the performance. The system equation of a 6^{th}-order MSCL modulator is calculated in appendix I. In [58], it is shown that the performance of MSCL structures is closely similar to the MASH performance. This structure is rediscovered in [59] and [60] and is renamed as SMASH (Sturdy MASH) structures.

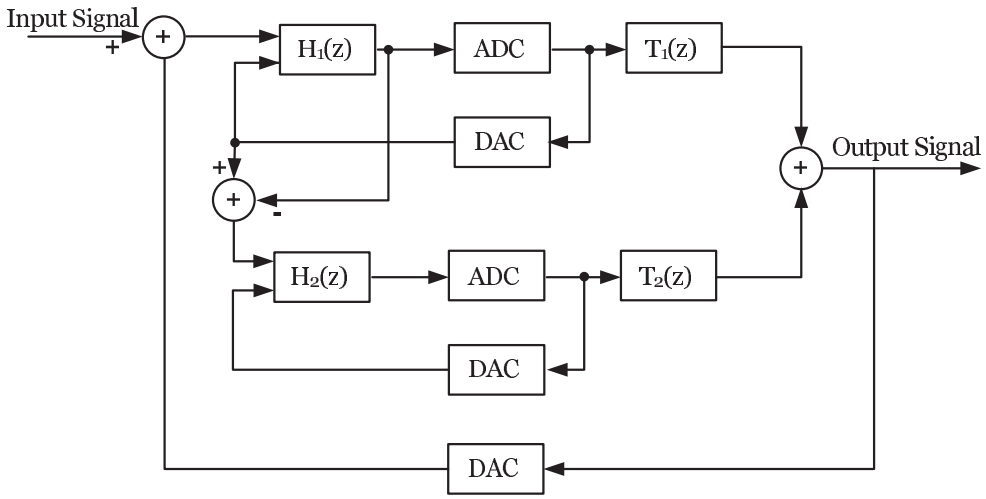

Figure 2.19: Second-order MSCL topology.

2.3.2 Single-stage modulators

2.3.2.1 Multi-feedback structures

A 6^{th}-order multi-feedback structure is presented in figure 2.20. A sufficient number

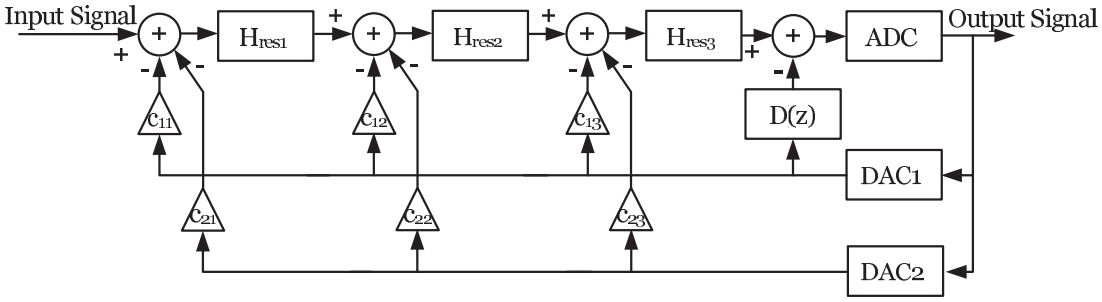

Figure 2.20: 6^{th}-order multi-feedback structure.

of degrees of freedom are provided by c_{ij} coefficients to synthesize the global filter. In order to improve the control on the NTF poles position, two DACs in the feedback loops are chosen from different types (NRZ, RZ or HZ). A large number of coefficients and employing two DACs are the main disadvantages of this structure. However, since in the case of low-order modulator these disadvantages are less critical, this structure is efficient especially for the design of fourth-order modulators [62], [63].

2.3.2.2 Mono-feedback structures

In order to prevent the disadvantage of linear DACs, especially in high-order context, mono-feedback structures are an alternative. The structure contains only one feedback loop as it is shown in figure 2.21, but the provided number of coefficients (c_i) is insufficient to synthesize the global filter. As a result, the following resonator transfer function must be employed.

$$H_{res} = \frac{a_i s + b_i}{s^2 + \frac{\omega_i}{Q} s + \omega_i^2}. \tag{2.19}$$

In fact, b_i in the numerator of H_{res} is introduced as a modifiable coefficient for providing a sufficient number of degrees of freedom. However, in chapter III, it is shown that this term is a characteristic of the classical resonators (RLC, Gm-C, Gm-LC and etc) produced because of parasitic resistors. Therefore this term is generally imposed by the manufacturing process and it is not possible to employ it as a modifiable parameter.

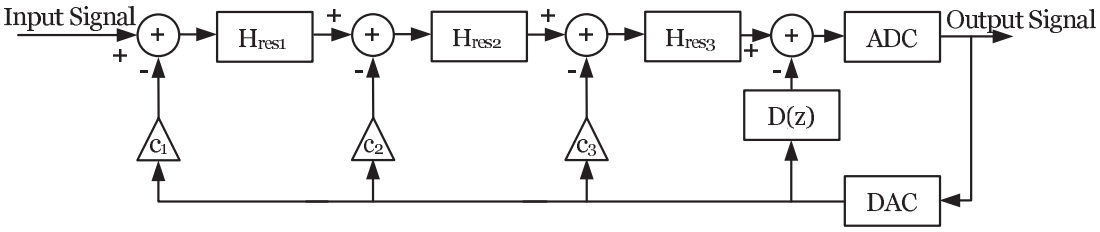

Figure 2.21: 6^{th}-order mono-feedback structure.

2.3.2.3 Weighted feedforward structures

The global loop filter transfer function can be also synthesized by using feedforward structures (figure 2.22) rather than feedback structures [64], [65], [66], [67], [68]. Although this structure contains a unique DAC with a unique feedback path and a larger number of degrees of freedom compared with mono-feedback structures, the number of degree of freedom is still insufficient for an exact synthesis. This structure is advantageous in terms of chip area and power consumption compared with multi-feedback structures.

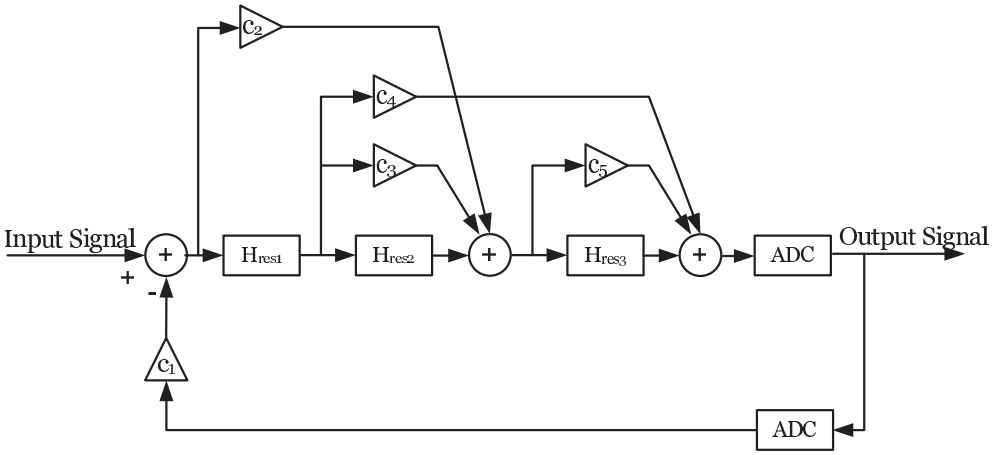

Figure 2.22: 6^{th}-order feedforward structure.

2.4 Performance criteria

The performance of a $\Sigma\Delta$ modulator is determined by both the resolution criteria and the stability criteria. A modulator performing a large resolution and a small stability margin is an efficient modulator in theory but not in practice. CT modulators are sensitive to analog non-idealities and manufacturing imperfections and such a modulator is very likely to become unstable in reality. In fact, an efficient $\Sigma\Delta$ modulator is a modulator performing the desired resolution with a large stability margin.

2.4.1 Resolution criteria

Several criteria exist to evaluate the modulator resolution. The most well-knowns are explained in this section.

2.4.1.1 Signal to noise ratio

This is the most used criterion describing the modulator resolution. The Signal to Noise Ratio (SNR) may be calculated by the following equation:

$$\mathrm{SNR}_{dB} = 10\ \mathrm{Log}_{10}\left(\frac{P_{\mathrm{signal}}}{P_{\mathrm{noise}}}\right), \tag{2.20}$$

where P_{signal} is the input signal power and P_{noise} is the noise power in the frequency band of interest. P_{signal} depends on the input signal amplitude and the presented SNR

in studies is the SNR obtained for a full-scale range of the input signal (SNR_{max}).

2.4.1.2 Bit resolution

The bit resolution or the effective number of bits (ENOB) presents the quantization number of bits of a classic Nyquist-rate converter performing at the same resolution as the ΣΔ modulator. The ENOB is computed from the SNR by the following equation:

$$\text{SNR}_{dB} = 6.02N + 1.76, \tag{2.21}$$

where N represents the ENOB. It should be noted that the ENOB is also calculated for a full-scale range of the input signal.

2.4.1.3 Signal to noise and distortion ratio

The Signal to Noise and Distortion ratio (SNDR) also takes into account the influence of harmonics on the modulator performance. It is given by:

$$\text{SNRD}_{dB} = 10 \text{ Log} \left(\frac{P_{\text{signal}}}{P_{|\text{noise+distortion}|}} \right). \tag{2.22}$$

Computing the SNDR is difficult through classical analysis because the quantizer is replaced by its linear model.

2.4.1.4 Input dynamic range

The input dynamic range is the difference, in dB, between the input amplitude for which the SNDR is equal to SNDR_{max}-3dB and the input signal for which the SNDR is equal to zero. In order to calculate the input amplitude for which SNDR is equal to SNDR_{max}-3dB, the input amplitude must exceed from the maximum input signal corresponding to SNDR_{max} (figure 2.23).

2.4.2 Stability criteria

The design of a ΣΔ modulator is not finished unless a robust stability condition is obtained. Although many studies have been done to find a reliable criterion of stability [69], [70], [71], [72], [73], [74], they give no guarantee for stability. The main reason is that, a ΣΔ modulator is a highly non-linear system because of the presence of a

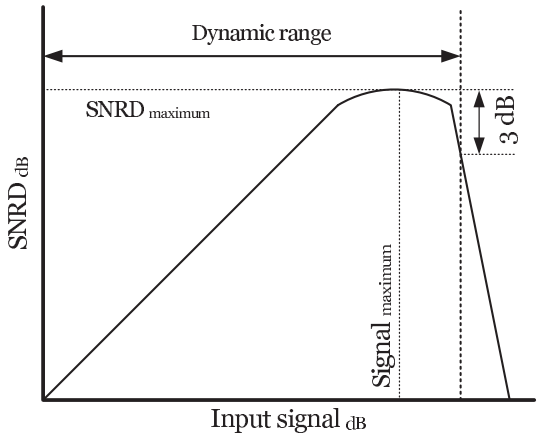

Figure 2.23: Concept of the input signal dynamic range.

low-order quantizer. In the context of ΣΔ modulators, the quantizer input signal and the quantization noise are chaotic signals and an analysis of non-linear system with random excitation is needed. The stability analysis of a closed-loop highly non-linear system with random excitation has always been an issue [75]. Usually, the stability analysis is done by making a linear approximation of the non-linear part to find an approximate equivalent predicting the response of the non-linear system.

Studying the stability is more critical for high-order modulator than low-order ones because they are potentially unstable. It is not possible to establish an unconditional stability regime of a high-order modulator and we are just looking for reducing the chance of instability of high-order ΣΔ modulators by satisfying different stability criteria. It should be noted that without extra enhancements, once the modulator is gone to the instability zone it cannot come back to the stability zone unless by an external reset. When the quantizer gain is smaller than the quantizer gain in the linear stable region, the modulator is gone to the instability zone and it can not be recovered because the negative feedback is changed to a positive one [76]. The modulator then starts to oscillate. In fact, the quantizer input represents the sum of long term quantization errors. When the quantizer input is low, which corresponds to a high quantizer gain in the linear model (figure 2.5), the modulator output corresponds to the input signal and no information is lost.

2.4.2.1 Bounded input-bounded output criterion

Regarding the Bounded Input Bounded-Output (BIBO) criterion [72], a ΣΔ modulator is stable if the closed-loop transfer function output is bounded for every bounded input and it is totally unstable if the oscillation moves toward the saturation zone for a null input signal.

2.4.2.2 Lee criterion

This is one of the widely used approximate criterion in ΣΔ modulator design. A binary ΣΔ modulator is likely to be stable if [77], [78]:

$$\left|NTF(e^{j\omega})\right| < 1.5. \tag{2.23}$$

This criterion is neither necessary nor sufficient because the criterion says nothing about the limits of the input signal [79]. Nevertheless, due to its simplicity, it is of some use.

2.4.2.3 Classical stability margins

The modulus (m), gain (k) and phase (φ) margins, corresponding to different geometrical terms characterizing the distance between the Nyquist plot of the open-loop transfer function ($\widehat{F}(z)$) and the critical point $[-1, j0]$, are defined in figure 2.24.

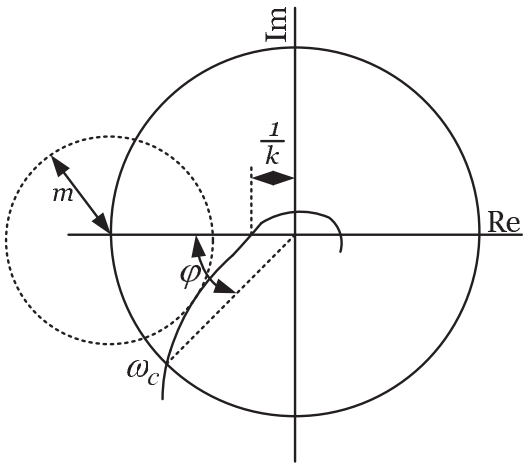

Figure 2.24: Modulus, gain and phase margin for the open-loop frequency characteristic.

Stability margins are used to assess the stability limits of closed loop systems on the Nyquist plot of the open-loop transfer function. The Nyquist plot allows to understand the influence of the modeling errors and to derive appropriate specifications to assume a robust stability of the closed-loop [80]. In the context of ΣΔ modulators, these margins are quasi-reliable when the linear model of the modulator is justified, in other word, when the modulator is a high-order one or contains a high-order quantizer. Satisfying classical margins are necessary but not sufficient to guarantee the stability of the modulator.

The definition of gain and phase margins are explained in any classical control hand books. The focus, in the present work, is on the definition of modulus margin which is defined as the radius of the circle centered in $[-1, j0]$ and the tangent to the Nyquist plot of $\widehat{F}(z)$ [81]. It results in:

$$\begin{aligned} m &= \min\left\{\left|1+\widehat{F}(e^{j\omega})\right|\right\} = \min\left\{\left|S^{-1}(j\omega)\right|\right\} \\ &= \left(\max\left\{|S(j\omega)|\right\}\right)^{-1} = \left(\|S(j\omega)\|_{\infty}\right)^{-1}. \end{aligned} \tag{2.24}$$

Modulus margin covers the gain and phase margins informations and is a number which can be a comprehensible reference to compare the stability and the sensitivity of different circuits. It is preferable that the sensitivity to analog parameters be as small as possible. Therefore, the modulus margin should be as large as possible. In the present work, this margin is considered as one of the most substantial parameters in the design of CT modulators.

The linear DT closed-loop model of the CT modulator (figure 2.25) is used to

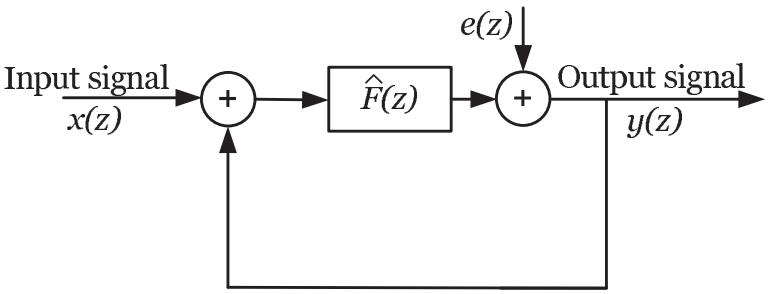

Figure 2.25: Required DT linear model of CT modulators for calculating the stability margins.

calculate the classical margins because the input signal, the output signal and the

global filter are in a same domain. The main issue is how to find the linear DT model (figure 2.25) of a CT modulator. The problem consists in finding a $\widehat{F}(z)$ making the equivalence between the topology of figure 2.26 and the topology of figure 2.25 regardless of the employed structure to synthesize $G(s)$. According to the topology of figure 2.26 which is is another representation of the topology of figure 2.16, the relation between $x^*(z)$, $e(z)$ and $y(z)$ is given by:

$$y(z) = e(z)\frac{1}{1+D(z)} + x(z)\frac{1}{1+D(z)}. \tag{2.25}$$

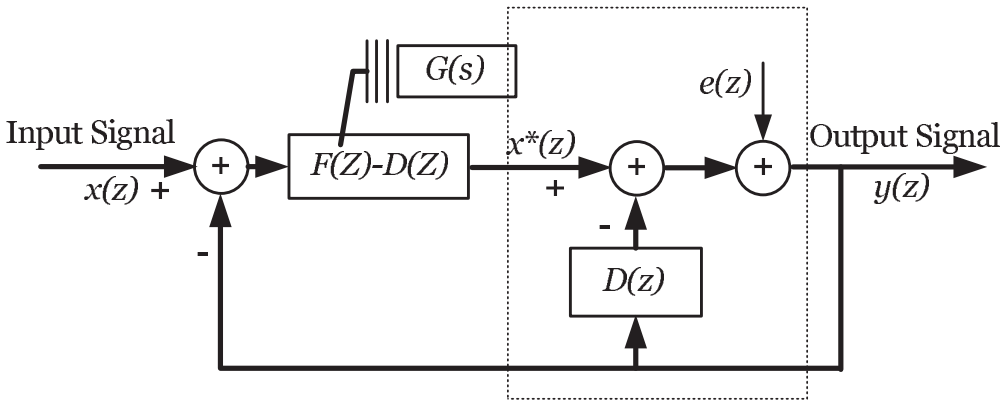

Figure 2.26: Another representation of figure 2.16 .

This means that the feedforward path signal and the quantization noise are both processed by a filter in the form of $\frac{1}{1+D(z)}$. Then the dotted part of figure 2.26 can be replaced as it is shown in figure 2.27

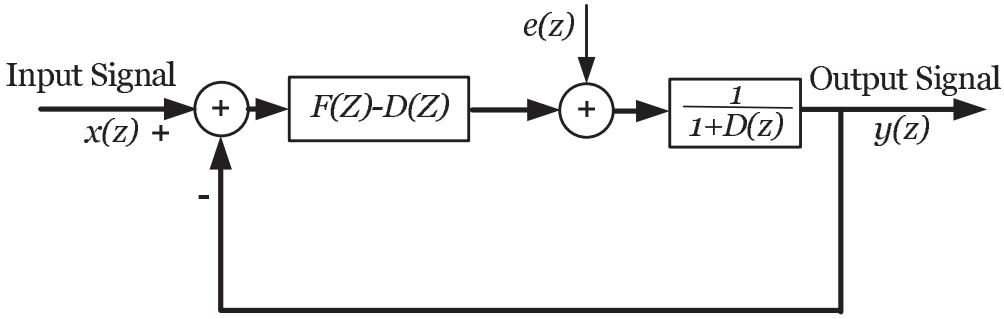

Figure 2.27: First step to find the linear DT mono-loop model.

The system modification done in figure 2.28 (replacing the $\frac{1}{1+D(z)}$ filter) is also permitted by control theories.

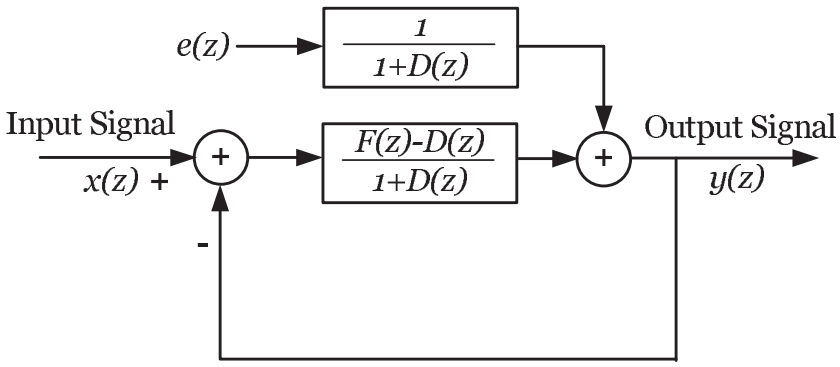

Figure 2.28: DT linear model of CT modulators to calculate the modulus margin.

Hence, $\widehat{F}(z)$ must be equal to:

$$\widehat{F}(z) = \frac{F(z) - D(z)}{1 + D(z)}. \tag{2.26}$$

The system equation of figure 2.26 is given by:

$$y(z) = x(z) \underbrace{\frac{F(z) - D(z)}{1 + F(z)}}_{STF} + e(z) \underbrace{\frac{1}{1 + F(z)}}_{NTF}. \tag{2.27}$$

Also, the system equation of figure 2.28 is given by:

$$y(z) = x(z) \underbrace{\frac{F(z) - D(z)}{1 + F(z)}}_{STF} + e(z) \underbrace{\frac{1}{1 + F(z)}}_{NTF}. \tag{2.28}$$

By comparing equation 2.27 with equation 2.28, the equivalence between the STF and the NTF of figure 2.26 and figure 2.28 is approved. As a result, the stability characteristics of both systems are the same.

2.5 Sigma-delta modulators history and trends

$\Sigma\Delta$ modulators are based on the Delta conversion principle [82]. The first ones were published by Spand and then Inose in 1962 for shaping the quantization noise in the

context of video signal transmission [83], [84]. Although the application of ΣΔ modulators in ADCs domain had been payed attention thanks to their efficiency [85], [86], [87], the first monolithic integrated ΣΔ modulator was presented in 1981 when the ability of integration of mixed-signal circuits (CT and DT circuits on the same chip) had progressed [88]. Afterward, the design of DT ΣΔ modulators has been rapidly progressed and they have taken the place of classical converters because of their high-resolution performance. For example, in audio applications, a resolution around 20-bits is easily achieved by them for a bandwidth between 24 KHz and 96 KHz[89], [90], [91], [92].

Nevertheless, the demands of new telecommunication systems for wide-band high-resolution ADCs are not satisfied by DT modulators and the studies are leaded to employ CT techniques. The first studies were based on the classical resonators like Gm-c resonators and Gm-LC resonators but they have never attained the required bit resolution in wide-band applications because of low quality factors and the sensitivity of the classical resonators to manufacturing process and temperature variations. Some important studies on CT ΣΔ modulators are listed in table 2.1.

Table 2.1: Comparison various studies on CT modulators employing the classical resonators

Reference	Resonator	ΣΔ order	f_s	f_c	Δf	SNR
[93]	Gm-LC	4	$4GHz$	$1GHz$	$20MHz$	$52dB$
[47]	Gm-C	2	$280MHz$	$70MHz$	$200KHz$	$45dB$
[62]	Gm-LC	4	$3.2GHz$	$800MHz$	$100KHz$	$66dB$
[94]	Gm-LC	4	$4GHz$	$1MHz$	$4MHz$	$53dB$
[49]	Gm-LC	2	$3.8GHz$	$950MHz$	$200KHz$	$57dB$
[95]	Gm-C	4	$4GHz$	$210MHz$	$1MHz$	$78dB$
[96]	Gm-LC	6	$1.2GHz$	$300MHz$	$4MHz$	$89dB$
[97]	Gm-C	4	$800MHz$	$200MHz$	$200KHz$	$68dB$
[63]	Active RC	6	$40MHz$	$10.7MHz$	$200KHz$	$63dB$
[48]	LC-SC	4	$400MHz$	$100MHz$	$200KHz$	$45dB$
[98]	Switched OpAmp	4	$10.7MHz$	$7.1MHz$	$200KHz$	$60dB$

The new trend in ΣΔ modulator design consists in employing micro-mechanical resonators as loop filter to avoid the issues of classical resonators. Although recent

progress has made possible the integration of micro-mechanical devices with CMOS circuits on a single chip, this kind of modulators is still immature [99], [100].

2.6 Conclusion

$\Sigma\Delta$ modulators are interesting when high-resolution and band-pass conversion are of primary importance. However their bounded bandwidth is the main disadvantage for wide-band applications. Although putting them in parallel is a solution in order to attain a wide-band A/D converter, the design of a proper $\Sigma\Delta$ modulator in this context meets various difficulties. Overcoming these difficulties is the main motivation of the present work. To this end, the principle of operation, the characteristics and the various methods of design of $\Sigma\Delta$ converters must be studied first.

The different classes of $\Sigma\Delta$ modulators (CT/DT, multi-stage/single-stage, etc) were presented and their relative advantages were discussed. It was shown that the sampling frequency of DT $\Sigma\Delta$ modulators is limited and that using CT methods is the only way to overcome this issue. However, working in the CT domain makes the design of CT modulators sensitive to coefficients errors. Single-stage techniques then become mandatory.

The performance of a high-order $\Sigma\Delta$ modulator is in general described by its resolution, stability, sensitivity to imperfections and linearity. Since an optimization method is developed in the present work to overcome the issues of high-order CT single-stage $\Sigma\Delta$ modulators, the need of comprehensible numbers to compare the performance of the designed modulator in different cases leads us to retain the modulus margin and the bit resolution as the representatives of the performance.

In the next chapter, $\Sigma\Delta$ modulators will be studied in the context of parallel conversion. It will be shown that some special characteristics are required to design a proper modulator for parallel conversion. These characteristics are extracted and the difficulties to attain them are then discussed. In the following chapters the proposed solutions to overcome these difficulties are explained.

3

Scope of Problem

A ΣΔ modulator working in the context of parallel A/D converters must satisfy extra specifications compared with conventional ΣΔ modulators. The EFBD solution is chosen to parallelize the modulators because it is less sensitive to analog imperfections compared with other counterparts. However, convenient modulators are required to ensure the performance of the EFBD. The requirements of EFBD systems are studied to extract the specifications of a convenient modulator.

3.1 EFBD requirements

3.1.1 Brief history

Extended frequency band decomposition is an improved system based on the frequency band decomposition principle. Understanding the FBD systems is therefore necessary for describing the EFBD systems.

The FBD is based on filter bank structures [101]. The solution consists in parallelizing ΣΔ ADCs working at different central frequencies (figure 3.1). The entire frequency band from 0 Hz into $\frac{f_s}{2}$ Hz is decomposed to N sub-bands and each of them is processed by the corresponding channel. The output of each modulator runs into a band-pass filter, centered on the modulator central frequency, to eliminate the out-of-band noise. The output of the band-pass filters are composed together to reconstruct the digitalized input signal.

Although FBD is less sensitive to analog imperfections (especially the gain of analog components), its main disadvantage is the complexity of the system [17]. The work-

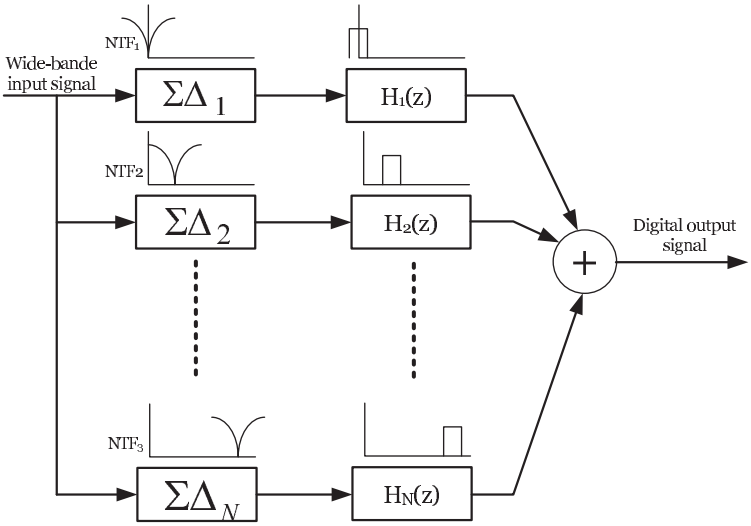

Figure 3.1: Frequency band decomposition principle.

band of FBD is extremely large while in most applications only a portion of this band is of interest. Band-pass FBD systems [20], employing N modulators to process the frequency band of interest, is an alternative to reduce the complexity of the system. The work-band of a band-pass FBD is smaller compared with FBD systems (figure 3.2). As a result, the frequency band of the modulators can be reduced to increase their resolution.

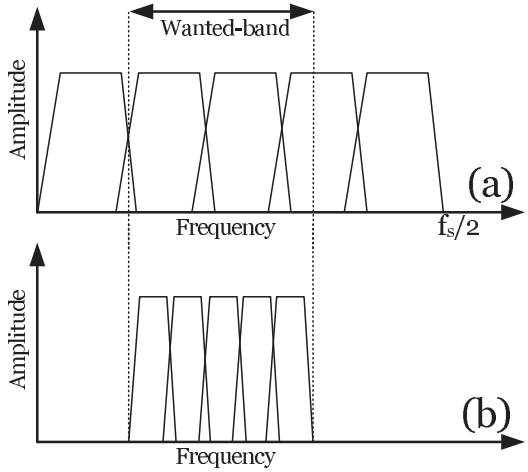

Figure 3.2: Comparison the work-band of a band-pass FBD system with that of a FBD system for $N = 5$.

Although band-pass FBD structures are less complex compared with FBD structures, they are sensitive to imprecision on the central frequency of the modulators. The work-band of a band-pass FBD system may move out from the input signal frequency band because of variations of the central frequency of the modulators. In [20] it is shown that for an error of the modulators central frequency equal to $20\%\frac{\text{work-band}}{N}$, a loss of resolution equal to 3-bits ocurres when the Q-factor of the filters is infinite.

EFBD systems propose solutions to reduce the sensitivity to the modulators central frequency imprecision [16], [19]. An EFBD contains $N+2$ parallel $\Sigma\Delta$ modulators (figure 3.3, analog part), where N is the number of modulators required to process the input signal band $[f1...f2]$. Two extra modulators are used in the case of large analog mismatches so that the wanted band $[f1...f2]$ remains within the work-band of the EFBD. The outputs of all channels are merged by a digital system (figure 3.3, digital part) to reconstruct the digitalized input signal [102].

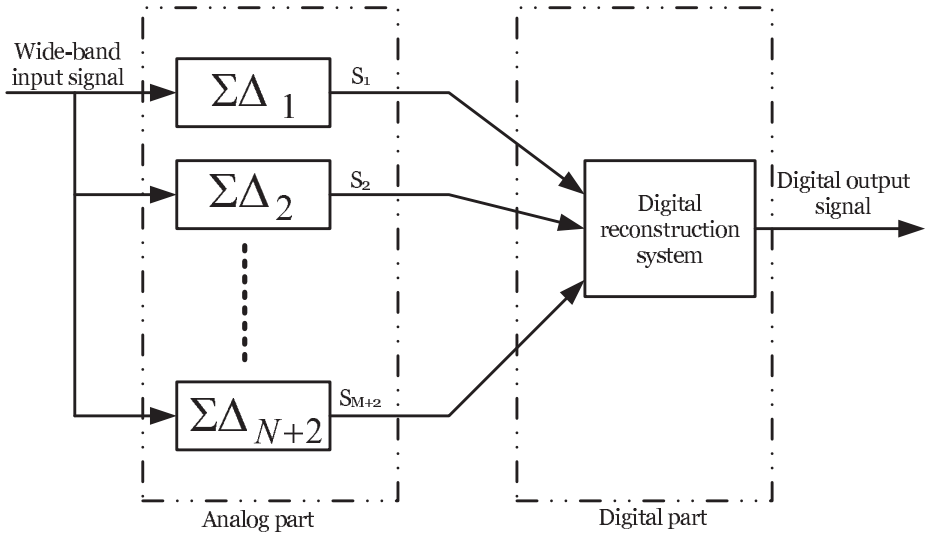

Figure 3.3: Extended frequency band decomposition principle.

The performance of the EFBD depends on the performance of the digital reconstruction algorithm and the performance of the analog part. The reconstruction algorithm is studied in [20] assuming that the analog part has an ideal performance. On the contrary, in the present work, the digital reconstruction algorithm is supposed as an ideal component and the NTF of the EFBD is calculated in function of analog part parameters.

3.1.2 In-band noise power of EFBD systems

A 6^{th}-order MSCL $\Sigma\Delta$ is chosen to calculate the in-band noise power of an EFBD system since the expression of its NTF is simple. The approximate NTF of a 6^{th}-order $\Sigma\Delta$ modulator based on MSCL is given by:

$$NTF(z) = \prod_{j=1}^{3} NTF_j(z) = \prod_{j=1}^{3} \frac{1}{1 + c_j \hat{H}_j(z)}, \tag{3.1}$$

where $\hat{H}(z)$ is the resonator transfer function in the z domain and c is the gain coefficient of resonators. This expression is obtained through the linear model of the modulator [103] and the calculations are demonstrated in appendix I. The transfer function of a band-pass resonator with a finite Q-factor in the s domain is expressed by:

$$H(s) = \frac{as + b}{s^2 + \frac{\omega_r}{Q} s + \omega_r^2}, \tag{3.2}$$

where $\omega_r = 2\pi f_r$ and f_r is the resonance frequency of the resonators. $\hat{H}(z)$ can be found through $H(s)$ by the poles conservation principle. The calculations are also demonstrated in appendix I. The resulting $\hat{H}(z)$ is given by:

$$\hat{H}(z) = \frac{0.5 p_j z^{-1} - z^{-2}}{1 - p_j(1 - \frac{\omega_r j}{2Q_j}) z^{-1} + (1 - \frac{\omega_{rj}}{Q_j}) z^{-2}}. \tag{3.3}$$

Assuming that the resonator Q-factor is sufficiently large, the modulus of the NTF can be approximated by using the first order approximation around the resonance frequency as follows:

$$\|NTF(z)\|^2 = \| \prod_{j=1}^{3} NTF_j(z) \|^2 = (4\pi)^6 \prod_{j=1}^{3} \frac{(f - f_{rj})^2 + (\frac{f_{rj}}{2Q_j})^2}{c_j^2}. \tag{3.4}$$

The noise power residual in the frequency band of interest (P_{NTF}) can be calculated through the module of the NTF. P_{NTF} is a comprehensible number to study the influence of analog parameters on the modulator performance. Note that the resolution of the modulator is a function of the modulator in-band noise. P_{NTF} can be found by the following equation:

$$P_{NTF} = \int_{f_1}^{f_2} \| \prod_{j=1}^{3} NTF_j(z) \|^2 \Gamma(f) df = \int_{f_c-\Delta(f)/2}^{f_c+\Delta(f)/2} \| \prod_{j=1}^{3} NTF_j(z) \|^2 \Gamma(f) df, \quad (3.5)$$

where f_c is the modulator central frequency and $\Gamma(f)$ is the noise density injected by the quantizer given by:

$$\Gamma(f) = \frac{1}{3 \times 4^B f_s}. \quad (3.6)$$

B and f_s are respectively the quantizer number of bits and the sampling frequency. The residual noise power in the work-band of the EFBD system (P_{total}) is the sum of the P_{NTF} of each modulator:

$$P_{total} = \sum_{k=0}^{N+1} P_{NTF^k} = \sum_{k=0}^{N+1} \left(\int_{f_{c^k}-\Delta(f)/2}^{f_{c^k}+\Delta(f)/2} \| \prod_{j=1}^{3} NTF_{j^k}(z) \|^2 \Gamma(f) \mathrm{d}f \right). \quad (3.7)$$

where N corresponds to the number of parallel channels. The following parameters are the most efficients in terms of the performance of the EFBD:

- Modulator central frequency (f_{c^k}). Imperfections of the modulator central frequency results in the inconsistency of the intervals between the wanted sub-bands and also reduces the modulator resolution. Although solutions are proposed in [20] to compensate for the resolution loss because of intervals inconsistency, the problem of modulator resolution loss subsists.

- Resonator Q-factor. Although increasing the Q-factor results in decreasing the in-band noise, a large Q-factor is in contrast with the requirements of wide-band applications. The influence of the Q-factor on the modulator performance must be studied in order to chose a convenient Q-factor compatible with requirements.

- Modulator order. The EFBD system may attain the modulator resolution in the ideal case. Therefore, the modulator resolution must at least be equal to the wanted resolution of the EFBD system. A convenient choice of the modulator order is indispensable for this aim.

- Modulator bandwidth (Δf). The chip area and the power consumption of the analog part of the EFBD system (figure 3.3) can be reduced by decreasing the number of parallel channels. For this aim, each channel must process a larger band of frequency,in other word, the modulator bandwidth must be increased to cover the work-band. However, increasing Δf results in increasing the in-band noise of each modulator, in other word, in decreasing the modulator resolution.

Manifestly, proper specifications of $\Sigma\Delta$ modulators must be defined to ensure the performance of the EFBD.

3.2 Specifications of modulator parameters

3.2.1 Modulator order

For a given OSR, a high-order modulator is able to perform a larger SNR compared with a low-order (second-order or fourth-order) one. According to equation 3.5, increasing the quantizer number of bits (B) results also in decreasing the modulator in-band noise (P_{NTF}). Figure 3.4 shows the variation of the bit resolution of a CT MSCL structure versus the modulator order for several values of the quantizer number of bits when the OSR is equal to 64.

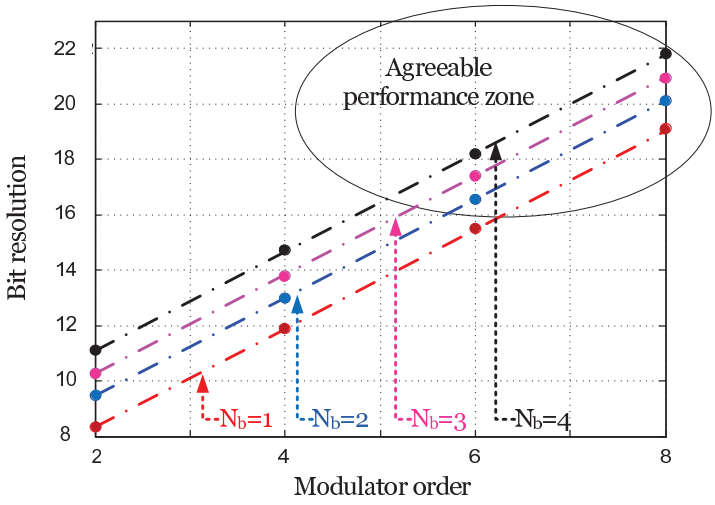

Figure 3.4: Variation of the modulator resolution versus the modulator order for several values of the quantizer number of bits when the OSR is equal to 64.

The wanted performance (bit resolution over than 16-bits) is achievable in two cases:

1. A 6^{th}-order modulator with a value of B larger than 2.

2. A 8^{th}-order modulator regardless of the value of B.

8^{th}-order modulators are most attractive whenever high SNR is important. Figure 3.4 shows that for the same quantizer number of bits, the resolution of an 8^{th}-order modulator is almost 3-bits larger than that of a 6^{th}-order modulator. The main obstacle to overcome is the issue of stability. 8^{th}-order modulators suffer seriously from instability issues while a 6^{th}-order modulator is a good compromise between resolution and stability [104]. To our knowledge, an implemented CT single-stage 8^{th}-order modulator has never been reported.

In order to attain the wanted resolution with a 6^{th}-order modulator, the quantizer number of bits must be larger than two. For small values of the quantizer number of bits, increasing the quantizer number of bits by one results in improving the modulator resolution by almost one-bit. However by passing from a 3-bits quantizer to a 4-bits quantizer, the improvement of the resolution is no more significant.
On the other side, the quantizer circuit becomes more complicated when increasing the quantizer number of bits. Note that in a $\Sigma\Delta$ modulator loop, the quantizer is a Flash A/D converter because of its high-speed performance. A Flash A/D converter contains $2^B - 1$ comparators to achieve a quantizer number of bits equal to B. Hence, a 4-bits Flash A/D converter almost doubles the occupied chip area and the power consumption compared with a 3-bits one.

As a result, a 6^{th}-order $\Sigma\Delta$ modulator with a 3-bits quantizer is able to attain the wanted resolution with the minimum of the issues of stability and chip area. The "additive white noise assumption" is also justified for a 6^{th}-order modulator [71].

3.2.2 Modulator bandwidth

According to equation 3.7, the in-band noise of the modulator is in inverse relation with Δf. Therefore, the resolution of the modulator becomes larger by reducing the modulator bandwidth. Considering the output noise spectrum density of a 6^{th}-order MSCL modulator, the power of the in-band noise increases exponentially by decreasing

the Over Sampling Ratio (OSR) of the modulator (figure 3.5). The relation between Δf and the OSR is given by:

$$\mathrm{OSR} = \frac{f_s}{\Delta f}. \tag{3.8}$$

In system-level simulations it is even possible to obtain the wanted resolution (16-bits) with a fourth-order modulator with an OSR equal to 400. However, in practice, the power of the in-band noise of the modulator cannot be diminished lower than the internal noise of electronic devices.

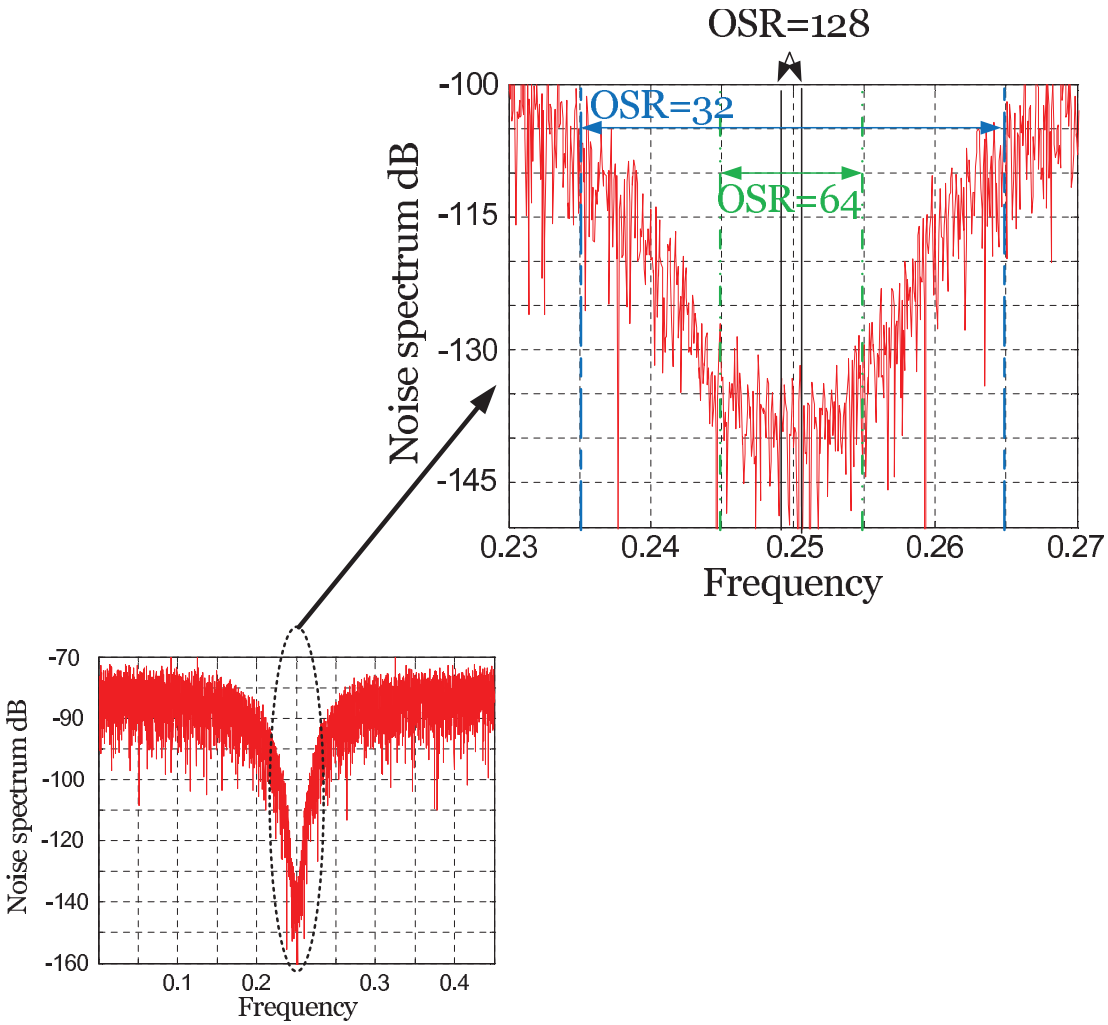

Figure 3.5: Output noise spectrum density of a 6^{th}-order CT MSCL working at $f_c = 0.25 f_s$.

On the other side, when reducing the bandwidth of the employed modulators, a larger number of modulators is required to cover the work-band of the EFBD. This results in increasing the occupied chip area and the power consumption of the EFBD system. In order to reduce them, the OSR of the modulator must be decreased.

Figure 3.6.a shows the evolution of the resolution of a 6^{th}-order CT MSCL $\Sigma\Delta$ modulator versus the modulator OSR. Figure 3.6.b shows the required number of modulators to cover the frequency band of interest ($0.2f_s < f < 0.3f_s$) versus the modulator OSR. The required resolution is achievable for an OSR larger than 50. Although an OSR equal to 100 results in increasing the bit resolution by 2-bits compared with an OSR equal to 50, the required number of modulators is also doubled. The OSR of the classical wide-band converters (equal to 64) seems to be a good compromise between the resolution and the required number of modulators.

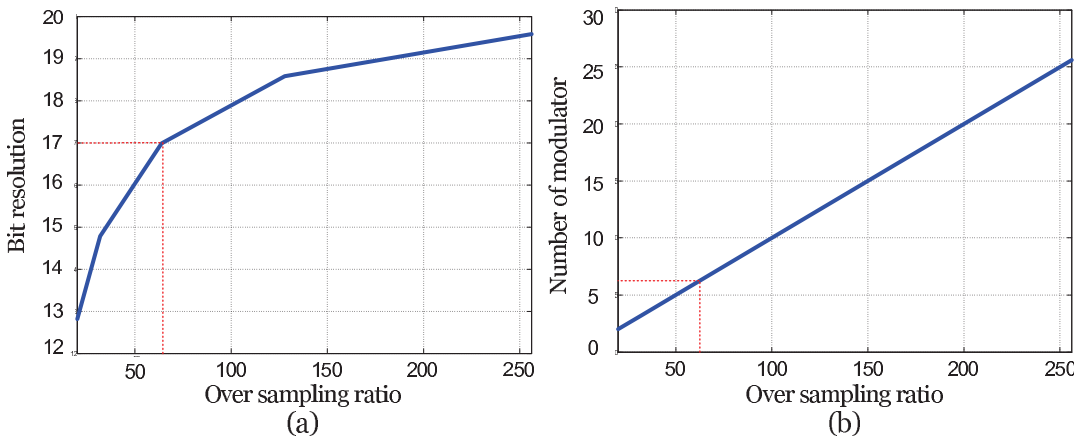

Figure 3.6: Modulator resolution (a) and required number of modulators (b) to cover the frequency band of interest ($0.2f_s < f < 0.3f_s$) versus OSR. The dotted line indicates the resulting resolution and the required number of modulators when OSR= 64.

3.2.3 Q-factor

Figure 3.7 shows the variation of P_{NTF} versus the modulator bandwidth for several values of the Q-factor for a 6^{th}-order CT MSCL working at $f_c = 0.25f_s$. Although increasing the Q-factor results in decreasing the in-band noise power, the variation ratio is more or less important depending on the modulator bandwidth.

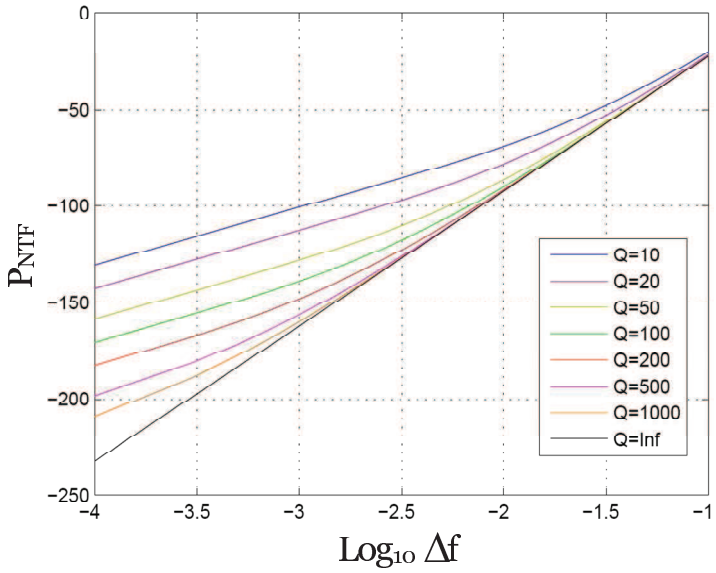

Figure 3.7: Variation of P_{NTF} versus the modulator bandwidth (Δf) for several values of the Q-factor.

Figure 3.8 illustrates the influence of the Q-factor on P_{NTF} when the OSR is equal to 64. The variation ratio of P_{NTF} for Q-factors less than 100 is significantly large

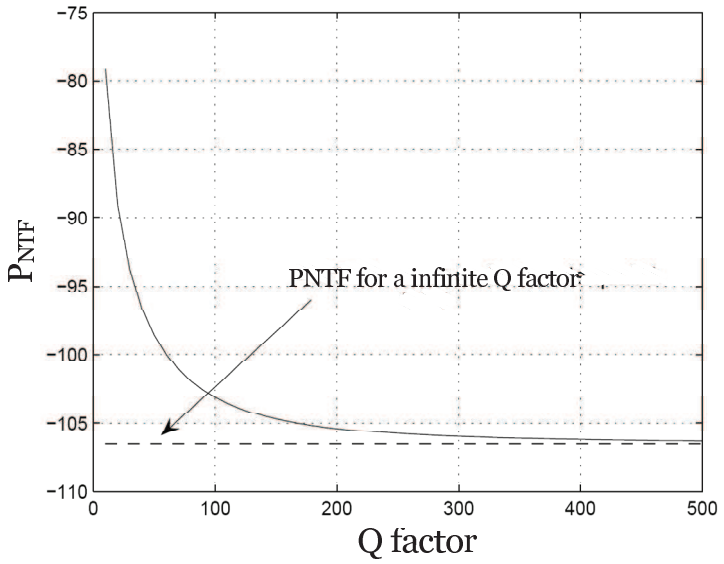

Figure 3.8: Variation of P_{NTF} versus Q-factors for an OSR equal to 64.

compared with Q-factors greater than 100. Although a large Q-factor ensures the performance of the modulator, it is in contrast with the requirements of wide-band applications. Therefore, a medium Q-factor around 100 seems to be a good compromise.

3.3 Specifications of resonators

An optimization factor of the resonance frequency of resonators (λ) for a 6^{th}-order modulator is defined as follows:

$$\lambda = \frac{|f_{r1} - f_{r2}|}{\Delta f} = \frac{|f_{r2} - f_{r3}|}{\Delta f}, \tag{3.9}$$

where f_{r1} and f_{r3} are the resonance frequencies of the side resonators and f_{r2} is the resonance frequency of the central on. The distances between the resonance frequencies of the side resonators and that of the central resonator are assumed equal. In the ideal case, f_{r2} is equal to the modulator central frequency (f_c). Assuming that Q-factor of the resonators is infinite, the in-band noise of the modulator (P_{NTF}) is given by [20]:

$$P_{NTF} = \left(\frac{4\pi}{c}\right)^6 \left(\frac{2(\Delta f)^7}{105}\right) (35\lambda^4 - 42\lambda^2 + 15)\Gamma(f). \tag{3.10}$$

When λ is equal to 0 (in other word all the resonators have the same resonance frequency equal to f_c), P_{NTF} can be simplified as follows:

$$P_{NTF} = \left(\frac{4\pi}{c}\right)^6 \left(\frac{2(\Delta f)^7}{7}\right) \Gamma(f), \tag{3.11}$$

while the optimal value of λ to minimize P_{NTF} is equal to $\sqrt{\frac{3}{5}}$ [105]. Then P_{NTF} is given by (to be compared with equation 3.11):

$$P_{NTF} = \left(\frac{4\pi}{c}\right)^6 \left(\frac{2(\Delta f)^7}{175}\right) \Gamma(f). \tag{3.12}$$

The variation of P_{NTF} versus λ is shown in figure 3.9 for an OSR equal to 64. A large error of λ, because of imprecision of the resonance frequency of resonators, results in a large deterioration of the modulator resolution. Imprecision of the resonance frequency of resonators is because of the sensitivity of resonators to the manufacturing process, temperature variations and non convenient impedances of connected electronic circuits.

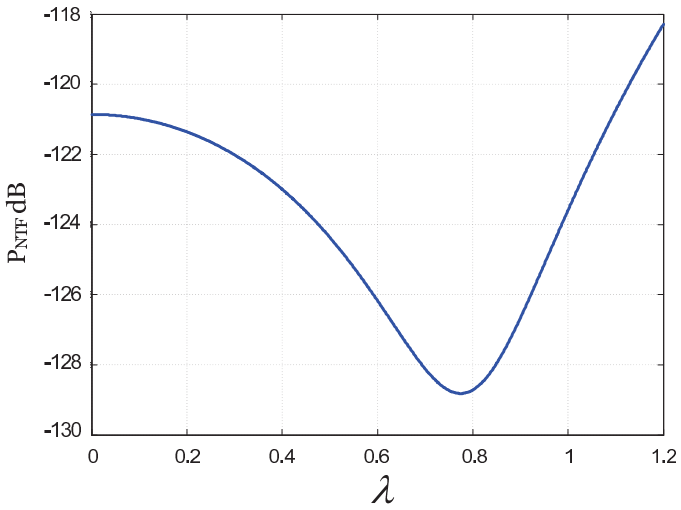

Figure 3.9: Variation of P_{NTF} versus λ.

Although the optimal λ may never attained, the resonator resonance frequency must be as immune as possible to these parameters.

The ideal transfer function of a second-order band-pass resonator with a finite Q-factor is given by:

$$H_i(s) = \frac{bs}{s^2 + \frac{\omega_r}{Q}s + \omega_r^2}. \tag{3.13}$$

Because of parasitic parameters its practical transfer function contains high-order polynomials in the numerator and in the denominator:

$$H_p(s) = \frac{b_0 + b_1 s + b_2 s^2 + ... + b_{i-1} s^{i-1}}{a_0 + a_1 s + a_2 s^2 + ... + a_i s^i}. \tag{3.14}$$

The extra poles and zeros are the representatives of harmonic contents and anti-resonances. The influence of them on the resonator performance can be reduced by a proper electronic control circuit. However, the existence of a constant term in the numerator may cause several issues on the design of the electronic control circuit in DC-level since the resonator is not anymore an open-circuit at DC. In order to avoid these kinds of issues, a structure able to present a real band-pass transfer function (without constant term in the numerator) is always preferred.

3.4 Specifications of modulator topology for high-loop-delays

3.4.1 NTF implementation

Regardless of the used method to synthesize the global filter transfer function ($G(s)$), the implementation of the topology of figure 2.17 faces several problems because of the method employed to implement $D(z)$.

The intermediate terms of $D(z)$ corresponding to a delay value larger than the ADC delay but less than the loop delay (ADC+DAC delay) are implemented by a fast DAC. The performance of high-order $\Sigma\Delta$ modulators is sensitive to the DAC performance while fast DACs are generally non-linear components.

The first terms of $D(z)$ corresponding to a delay value less than the ADC delay are implemented through the sampler output. Because of the sampling function, the implementation of $T_1(z)$ is only feasible with switched-capacitor or switched-current techniques. The speed of these techniques are bounded which results in limiting the modulator speed. Moreover, making a direct feedback from the sampler output to its input without passing through the modulator global filter ($G(s)$), injects a part of the sampler noise directly to the forward path.

The topology of figure 3.10 is another representation of that of figure 2.17. The A/D

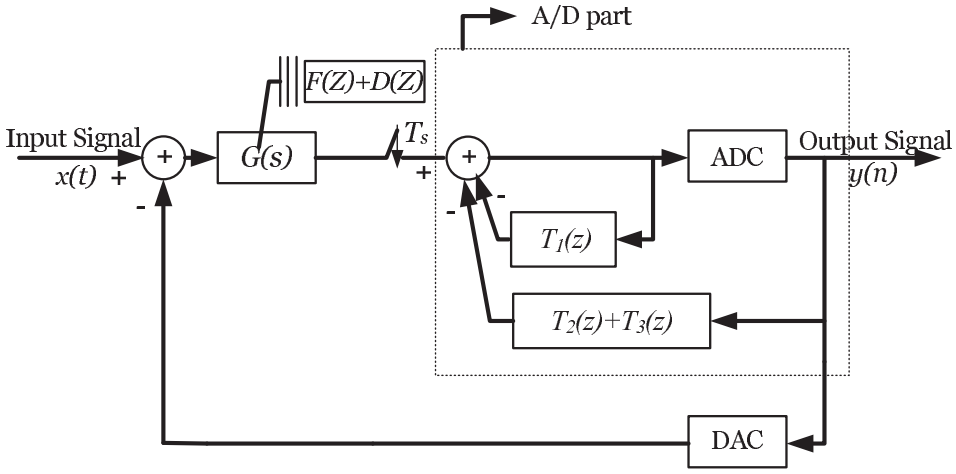

Figure 3.10: Another representation of figure 2.17.

part may be simplified by using the linear model of the ADC. This leads in illustrated

topology in figure 3.11.

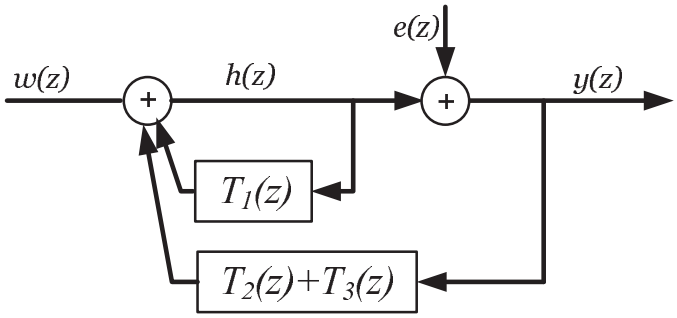

Figure 3.11: Linear model of the A/D part of figure 3.10.

Then, the relation between $w(z)$, $h(z)$ and $y(z)$ is given by:

$$h(z) = T_1(z)h(z) + w(z) + (T_2(z) + T_3(z))y(z). \tag{3.15}$$

Moreover, the output signal ($y(z)$) can be defined as a function of $e(z)$ and $h(z)$:

$$y(z) = e(z) + h(z). \tag{3.16}$$

Substituting $h(z)$ from equation 3.15 into equation 3.16 gives a new expression of $y(z)$:

$$y(z) = w(z)\frac{1}{1 - T_1(z) - T_2(z) - T_3(z)} + e(z)\frac{1 - T_1(z)}{1 - T_1(z) - T_2(z) - T_3(z)}. \tag{3.17}$$

The DT equivalent model of figure 2.17, deduced from equation 3.17, is presented in figure 3.12.

The NTF and the STF expressions of the topology of figure 3.12 are:

$$y(z) = \underbrace{\frac{1 - T_1(z)}{1 + F(z)}}_{NTF} e(z) + \underbrace{\frac{F(z) + D(z)}{1 + F(z)}}_{STF} x(z), \tag{3.18}$$

where $D(z)$ is given by:

$$D(z) = \sum_k a_k z^{-k} = T_1(z) + T_2(z) + T_3(z). \tag{3.19}$$

A comparison with the NTF and the STF of the original DT modulator given by:

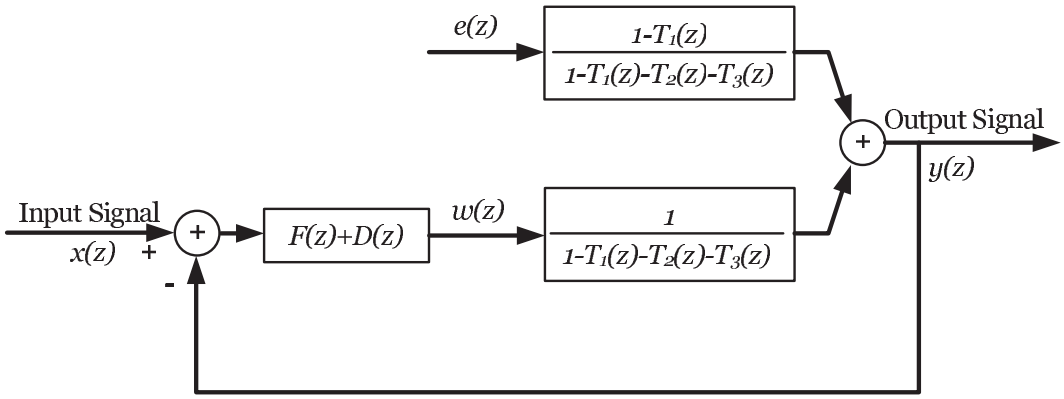

Figure 3.12: DT equivalent model of figure 2.17.

$$y(z) = \underbrace{\frac{1}{1+F(z)}}_{NTF} e(z) + \underbrace{\frac{F(z)}{1+F(z)}}_{STF} x(z), \tag{3.20}$$

shows that the method proposed to implement $D(z)$ changes the modulator performance. The modulus of the numerator of the NTF of equation 3.18 ($\|1 - T_1(z)\|$) is studied to evaluate the influence of the method employed to implement $T_1(z)$ on the NTF. Figure 3.13 shows the variation of $\|1 - T_1(z)\|$ versus the modulator central frequency ($0.2 < f_c < 0.3$) and the loop delay ($1T_s$ <delay< $2.5T_s$). A discontinuity for a delay value of $2T_s$ expected, $\|1 - T_1(z)\|$ is independent to the loop delay. However, the influence of $T_1(z)$ is more important for loop delays larger than $2T_s$ compared with loop delays less than $2T_s$. This is one of the reasons for which we intend to work with a loop delay between $1T_s$ and $2T_s$.

On the other side, $\|1 - T_1(z)\|$ depends on the modulator central frequency, in other word, the performance of the proposed structure in figure 2.17 depends on the modulator central frequency regardless of the used topology to synthesize $G(s)$. Although this is in contrast with the requirements of an EFBD system, an alternative method to implement $T_1(z)$ does not exist. One may eliminates them in order to release the design from practical issues (such as fast DAC implementation and switched-capacitor techniques) though the resulting performance deterioration.

This is a possible solution especially when the loop delay is between $1T_s$ and $2T_s$. According to the form of $D(z)$ for a loop delay between $1T_s$ and $2T_s$:

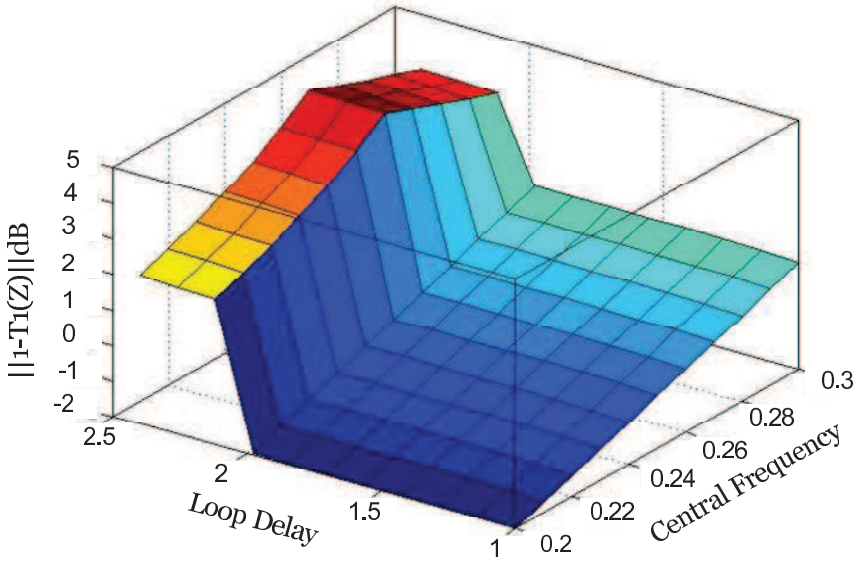

Figure 3.13: Variation $\|1 - T_1(z)\|$ in dB versus f_c $(0.2 < f_c < 0.3)$ and loop delay $(1T_s < \text{delay} < 2.5T_s)$.

$$D(z) = a_1 z^{-1} + a_2 z^{-2}, \tag{3.21}$$

$a_2 z^{-2}$ is implemented by T_3 and $a_1 z^{-1}$ is removed by this solution. The inserted error to the NTF because of removing $a_1 z^{-1}$ is not critical.

Now, assuming that the the loop delay is between $2T_s$ and $3T_s$. Although the design of the DAC becomes easier because a longer time is available to implement correction methods to linearize the DAC, the modulator performance is more deteriorated by the proposed solution. The new form of $D(z)$ when the loop delay is between $2T_s$ and $3T_s$ is given by:

$$D(z) = a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3}. \tag{3.22}$$

Only the last term of $D(z)$ is implemented by T_3 and others ($a_1 z^{-1}$ and $a_2 z^{-2}$) are removed by this solution. The inserted error to the NTF is very large and may results in instability for the modulator central frequencies close to $0.3 f_s$. This is the second reason for which we intend to work with a loop delay between $1T_s$ and $2T_s$.

Eliminating $T_1(z)$ and $T_2(z)$ leads to the topology of figure 3.14. Note that for $f_c = 0.25f_s$, the terms of $D(z)$ are all zero except the last and the proposed topology in figure 3.14 is exact.

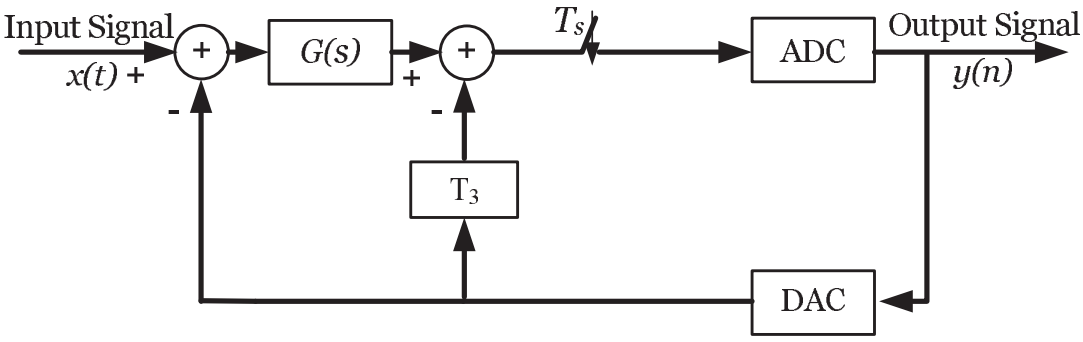

Figure 3.14: Topology obtained by removing $T_1(z)$ and $T_2(z)$.

3.4.2 Dealing with frequencies other than $f_c = 0.25f_s$

Figure 3.15 shows the variation of a_1 and a_2 (equation 3.21) versus the modulator central frequency for a 6^{th}-order $\Sigma\Delta$ modulator with a loop delay equal to $1.5T_s$. $|a_1|$ is equal to zero when $f_c = 0.25f_s$ but increases substantially when f_c moves from $0.25f_s$.

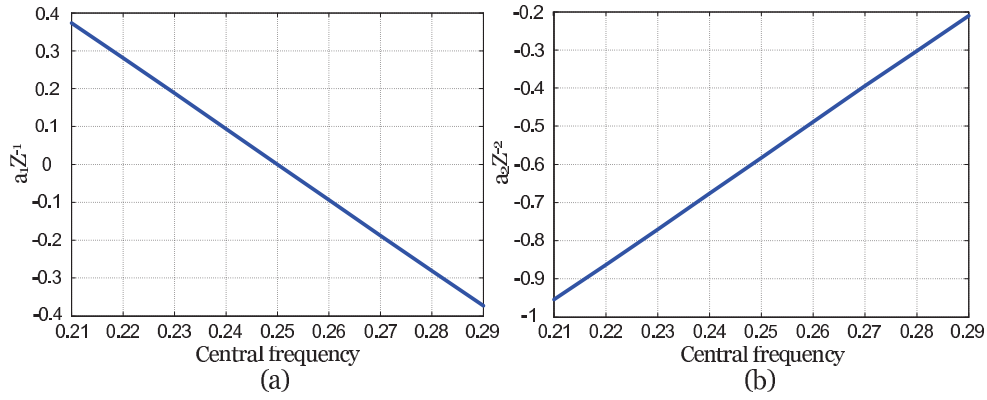

Figure 3.15: Variations of a_1 and a_2 (equation 3.21) versus the modulator central frequency.

The resolution and the modulus margin of the proposed topology (figure 3.14) is illustrated in figure 3.16 and compared with those of the original DT modulator. The

resolution of the modulator is unchanged since the absence of $T_1(z)$ results in variations of the NTF poles and not the NTF zeros. Note that the stability of the modulator is related to the position of the NTF poles and the resolution is related to the position of the NTF zeros. The modulus margin of the proposed topology is a function of the modulator central frequency and is significantly deteriorated close to the frequency band edges ($0.2f_s$ and $0.3f_s$). Therefore a simple synthesize of $G(s)$, whatever the used structure, is not reliable in terms of stability.

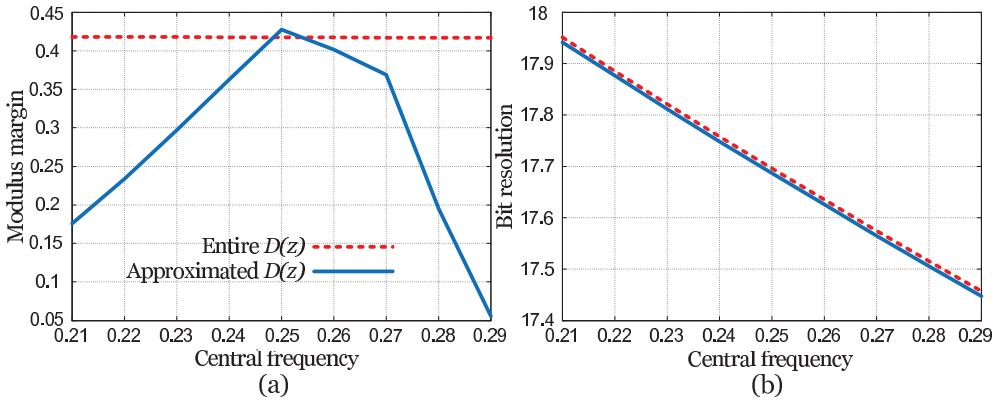

Figure 3.16: Modulus margin (a) and bit resolution (b) of the proposed topology compared with those of the original DT modulator, versus central frequency.

One may propose to modify $G(s)$ in order to compensate for the introduced error to the NTF because of the absence of $T_1(z)$. A proper topology to synthesize $G(s)$ offering an adequate control on the position of the NTF poles is then required. An optimization method must be also developed to re-define the parameters of the structure of the global filter.

3.5 Specifications of STF

In practical applications, the input signal of the A/D converter usually contains both the desired frequency band and a wide spectrum of interferer. Consequently, due to interferer, the dynamic range of the modulator is reduced. Filtering the input signal using a high-order filter is a solution to diminish the input interferer into the converter. This is not a favored solution in terms of chip area and power consumption because of

the requirements of high-order filters. Another solution consists in designing a filtering-STF modulator. Then the power of the out-of-band frequencies is reduced by the modulator itself. As a result, it is possible to replace high-order input filters with low-order one.

For this aim, first an analytical method to calculate the STF is required [44]. Since the STF is a function whose input is CT and its output is DT, it is not possible to define it directly in the s or the z domain. Some system modifications are necessary for an exact calculation of the STF. Figure 3.17 explicits step by step the system modifications [21].

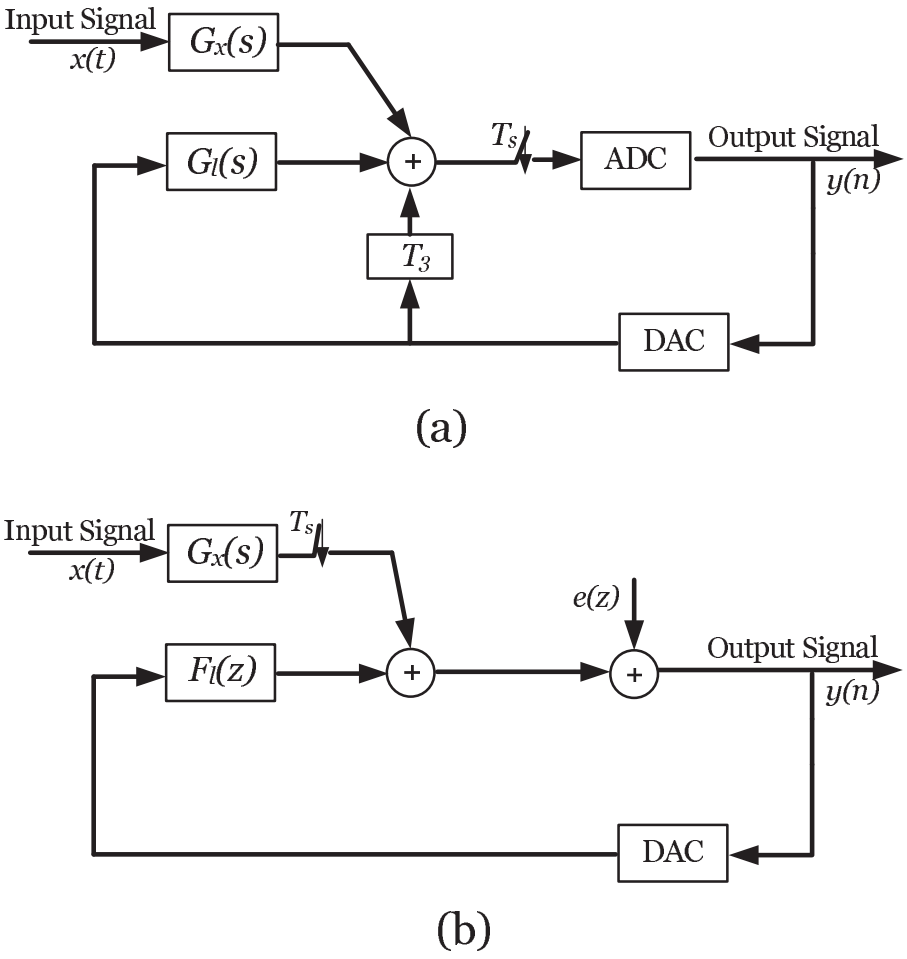

Figure 3.17: System modifications necessary to calculate the exact STF.

In the first step (figure 3.17.a) the modulator filter is divided into a forward-path

filter ($G_x(s)$) and a loop filter ($G_l(s)$). The second step consists in replacing $G_l(s)$ with its DT equivalent model since the samplers ensures a DT behavior of the loop filter. Then a sampler is placed in front of the forward-path filter to maintain the equivalence between figure 3.17.a and figure 3.17.b. The ADC is also replaced with its linear model. Through figure 3.17.b the input and the output signals of the NTF are in the z domain and its expression is given by:

$$NTF(z) = \frac{1}{1 - F_l(z)}. \tag{3.23}$$

On the contrary, there is no straightforward solution to calculate the expression of the STF in the s or the z domain. However, the STF can be calculated in the sense that an input signal at pulsation ω gives, after a possible aliasing, an output component at pulsation $\omega - 2k\pi f_s$, with $-\pi f_s < \omega - 2k\pi f_s < \pi f_s$:

$$STF(e^{j\omega T_s}) = \frac{G_x(j\omega)}{1 - F_l(e^{j\omega T_s})}. \tag{3.24}$$

In most conventional modulators, like the topology of figure 3.14, $G_l(s)$ and $G_x(s)$ are the same filters. Therefore, the global filter transfer function ($G(s)$) must be modified to change the STF [106] [107]. This is not a convenient solution because, as shown in the previous sub-section, strict constraints are imposed on $G(s)$ to attain the required NTF characteristics. Perceptibly, adding other constraints concerning the STF shaping would make the design impossible. Another solution, taken into account in this work, consists in making difference between $G_x(s)$ and $G_l(s)$. Then the STF can be modified without changing the NTF.

3.6 Conclusion

EFBD structures was chosen as a possible solution to parallelize modulators in order to widen the frequency band of converters since they are less sensitive to analog imperfections compared with other counterparts. However, the requirements of an EFBD system impose several specifications of a proper modulator.

It has been shown that an OSR equal to 64 is a good compromise between the required number of modulators to cover the bandwidth of the EFBD and the resolution of modulators. In order to attain the wanted resolution equal to 16-bits, a 6^{th}-order

modulator with a 3-bits quantizer was chosen. Although higher-order modulators are more attractive in terms of resolution, they face serious issues in terms of stability. It has been also shown that a Q-factor around 100 is a realistic value in the context of wide-band applications ensuring the modulator resolution.

A resonator able to provide the required Q-factor is needed. Moreover, the influence of the imprecision of the resonance frequency of resonators on the modulator performance was studied. It has been shown that a large imprecision results in a large deterioration of the modulator resolution. Hence, the employed resonator must be as immune as possible to manufacturing process and temperature variations.

In the present work, the global filter transfer function of a CT modulator is found through its DT equivalent by an z to s transform. It was shown that an exact practical implementation of the transform is not possible. Some terms have been removed in order to avoid practical issues and the loop delay has been considered between $1T_s$ and $2T_s$ in order to minimize the introduced error to the NTF. However, the stability margin of the proposed topology was became a function of the modulator central frequency and was deteriorated especially for the central frequencies close to the edges of the work-band. It is possible to compensate for the introduced error to the NTF by modifying the global filter transfer function.

Design of a filtering-STF modulator is also interesting to reduce the constraints on input filters of A/D converters. An analytical method to calculate the STF of a modulator was explained. It was also shown that for most of conventional modulators modifying the STF without changing the NTF is not possible. Since for a high-order modulator strict constraints on the NTF are imposed in order to attain a robust stability margin and to maintain the resolution, the STF shaping must be done without changing the NTF. Hence, extra solutions are required.

4

Lamb Wave Resonators

From the previous chapter, the required specifications of a suitable resonator, in the context of 6^{th}-order $\Sigma\Delta$ modulators are:

1. The ability of achieving the required Q-factor. In the context of a classical wide-band modulator with an OSR equal to 64, a Q-factor around 100 is required.

2. Pure band-pass resonator transfer function characteristics (equation 3.13).

3. Accurate resonance frequency with no need of tuning.

4. Good temperature stability.

5. A proper impedance at the resonance frequency. In order to ensure the performance of the resonator, the impedance of the corresponding electronic control circuit must be small compared with the resonator impedance at the resonance frequency. In practice, if the resonator impedance is too small, the design of the electronic control circuit faces serious problems.

The most well-known resonator types are studied in this chapter. It is shown that Lamb Wave Resonators (LWR) are the most appropriate in terms of resonance frequency range, Q-factor and compatibility with integration technologies. However, their performance suffer in general from the existence of an anti-resonance frequency. Solutions are proposed to overcome this issue.

4.1 Choice of resonator

Classical resonators (Gm-LC, Gm-C, etc), micro-mechanical resonators and piezo-electric resonators are studied in order to choose the most appropriate.

4.1.1 Classical resonators

4.1.2 Gm-LC resonators

Gm-LC resonators consists of integrated capacitances, inductances and a trans-conductance amplifier. Gm-LC resonators are more linear than the other classical resonators because of the possibility of applying linearization techniques to the trans-conductance amplifier. They have also two major disadvantages because of the integrated inductance. A large chip area is generally required for implementing the integrated inductance [108], [109]. Moreover, the parasitic resistance of the inductance deteriorates the resonator Q-factor [96]. Figure 4.1 presents a typical structure of a second-order Gm-LC resonator. The resonator transfer function is given by:

$$\frac{V_{out}}{V_{in}} = (\frac{g_m}{C}) \times \frac{s}{s^2 + \frac{g_m}{C}s + \frac{1}{LC}}. \tag{4.1}$$

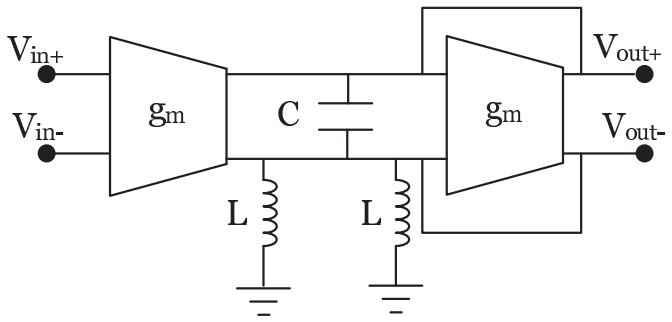

Figure 4.1: Structure of a typical second-order Gm-LC resonator.

4.1.3 Gm-C resonators

The integrated inductance of Gm-LC resonators can be replaced by an active inductance in order to decrease the surface of integration. This sort of resonators is known as Gm-C resonators. Although Gm-C resonators are compatible with various integration

technologies, their implementation faces serious problems for resonance frequencies over than 100 MHz. Because of the parasite capacitance and the looped structure, Gm-C resonators suffer, respectively, from resonance frequency imprecision and stability issues in high frequencies [110], [111]. A typical structure of a second order Gm-C resonator is presented in figure 4.2 [112]. The resonator transfer function is as follows:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{gm_1}{gm_2}}{1 + \frac{gm_3 C_1}{gm_2 gm_4} s + \frac{C_1 C_2}{gm_3 gm_4}}. \tag{4.2}$$

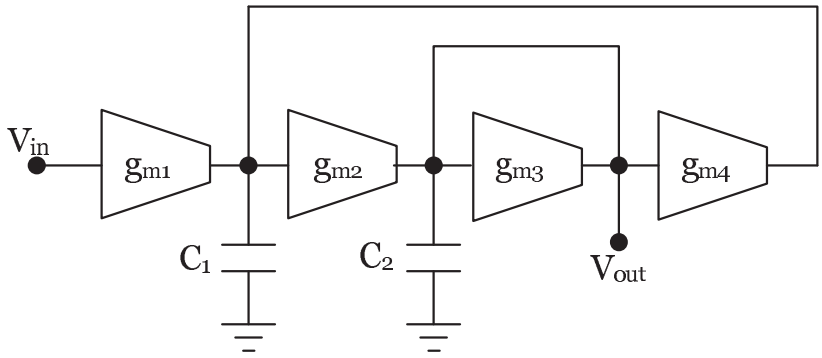

Figure 4.2: Structure of a typical second-order Gm-C resonator.

RC resonators [113], RONC-C resonators [114] and AOP-C resonators are other common kinds of classical resonators. The common disadvantage of these resonators is their low Q-factor. Q-enhancement circuits, based on negative resistors, are inevitable. However, Q-factor of these resonators does not exceed from 25 [115], [116]. When the value of the negative resistor is close to the resonator parasitic resistance, the resonator is close to instability zone. Moreover, Q-enhancement techniques deteriorate the linearity and the dynamic range of resonators. Another disadvantage of such resonators is the characteristics of the transfer function. Indeed they have not an open-circuit behavior at DC because of parasitic resistance resulting in the existence of b_0 in the numerator of equation 3.14. Hence, these resonators do not satisfy the specifications of a suitable resonator for $\Sigma\Delta$ modulator application.

4.1.4 Micro-mechanical resonators

The resonance, in the context of a micro-mechanical resonator (MEMS), is obtained via the vibration of a micro-machined. This principle is implemented by different structures

such as vibrating beam [117], square extensional [118], ring resonator [119], etc. Figure 4.3 shows the schematic view of a vibrating beam resonator.

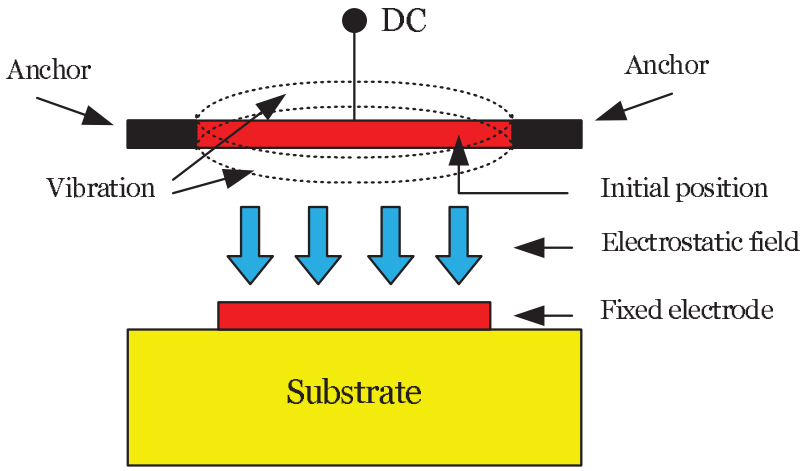

Figure 4.3: Schematic view of a typical vibrating beam MEMS.

MEMS are capable of high Q-factors (up to 170000) in a large frequency band but their major disadvantages are:

1. Micro-mechanical resonators are generally encapsulated in order to increase their Q-factor [120]. The encapsulation process is costly and not easily compatible with integration technologies.

2. They require a large biasing voltage between 10 V and 100 V, depending on off-chip [121] or on-chip [122] applications, in order to reduce the impedance at the resonance frequency. This range of biasing voltage is not permitted in low-consumption integrated circuits.

Indeed, the performance of MEMS resonators is interesting in terms of Q-factor [123] but the main issue is the integration problems on a low-cost low-consumption monolithic chip.

4.1.5 Piezo-electric resonators

A piezo-electric material like AlN and ZnO changes dimensions when it is exposed to an AC electric field. The frequency at which the piezo-electric vibrates most readily,

and most efficiently converts the electrical energy input into mechanical energy, is the resonance frequency. In the context of a piezo-electric resonator, the electrical field is produced by electrodes and the resonance frequency is set by determining the distance between them. Indeed, this distance must be equal to $\lambda/2$ where λ is the wave length of the produced electrical field and depends on the piezo-electric constants. The relation between λ and the resonance frequency is given by:

$$f_r = \frac{c}{\lambda}, \tag{4.3}$$

where c is the speed of the sound in the piezo-electric material.

Piezo-electric resonators are in general capable of a high Q-factor (up to 1000). Their resonance frequency is accurate and they are not very sensitive to temperature variation. Depending on the geometrical direction of the material vibration, they are classified in three different categorize.

4.1.5.1 Surface acoustic wave resonators

A surface acoustic wave (SAW) travels the surface of the piezo-electric material. The wave amplitude reduce exponentially with depth into the substrate. A typical structure of SAW resonators is shown in figure 4.4. the SAW wave propagate either towards

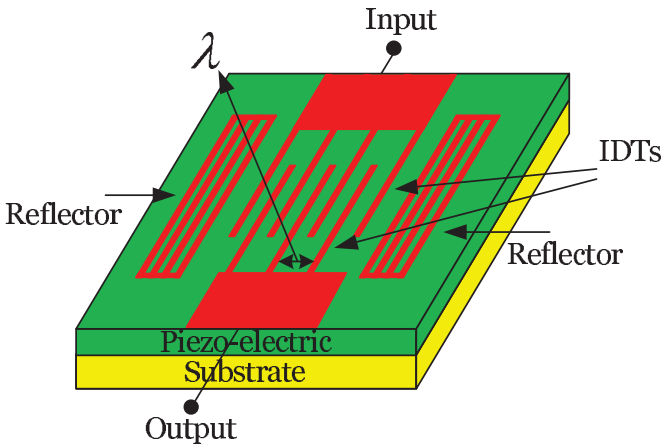

Figure 4.4: Schematic view of a typical SAW resonator.

reflectors and back to the Inter-Digital Transducers (IDTs) where it is converted back to electrical signal [124], [125]. The resonance frequency of SAW resonators in high

frequencies is limited by the lithography resolution [126]. However, they can operate at selected harmonic frequencies, depending on the metalization ratio (the relation between the IDT width and the distance between IDTs). SAW resonators are available for the resonance frequencies between 30 MHz and 2.7 GHz [127]. The main disadvantage is the direction of propagation of acoustic wave which is not compatible with piezo-electric deposition on a Si-substrate [128]. As a result the integration of SAW resonators is not easily done on a monolithic circuit and they are used in general as discrete components.

4.1.5.2 Bulk acoustic wave resonators

A Bulk Acoustic Wave travels the bulk of the piezo-electric material rather than the surface [129]. Then the propagation is compatible with piezo-electric deposition on a Si-substrate [128]. Although two common types of BAW resonators are reported, the piezo-electric material is confined between two electrodes regardless of the structure. In Solidly Mounted Resonators (SMR) structure (figure 4.5.a) the isolation between the piezo-electric layer and the substrate is made by a Bragg reflector while Film Bulk Acoustic Resonators (FBAR) structure (figure 4.5.b) is identical to the first one but the acoustic isolation is achieved by removing the silicon substrate underneath the active region of the resonator [130].

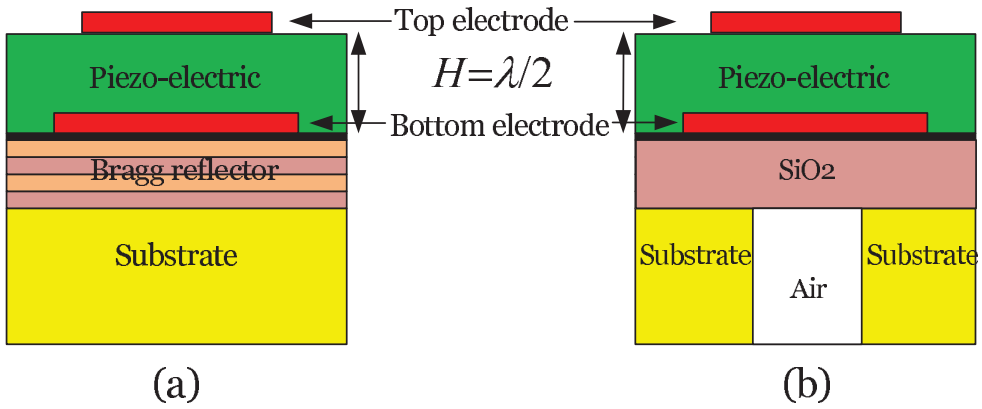

Figure 4.5: Schematic views of a typical SMR resonator (a) and a typical FBAR resonator (b).

The resonance frequency of BAW resonators is inverse by proportional to the material thickness (H). As an instance, the material thickness must be equal to 6 μm

to obtain a resonance frequency of 800 MHz for a simple structure [131]. Note that 6 μm is the largest possible thickness for most of the integration technologies. As a consequence, the resonance frequency of BAW resonators is limited between 800 MHz and 10 GHz [130]. Since the modulator sampling frequency, in this work, is equal to 400 MHz, BAW resonators are not convenient.

4.1.5.3 Lamb wave resonators

The velocity of lamb waves depends on the relation between the wavelength and the width of the material [132]. Lamb waves propagate in two symmetry and asymmetry modes shown in figure 4.6. Since the propagation is done in two dimension (X and y) the properties of a lamb wave is quite complex compared with bulk or surface acoustic waves [133].

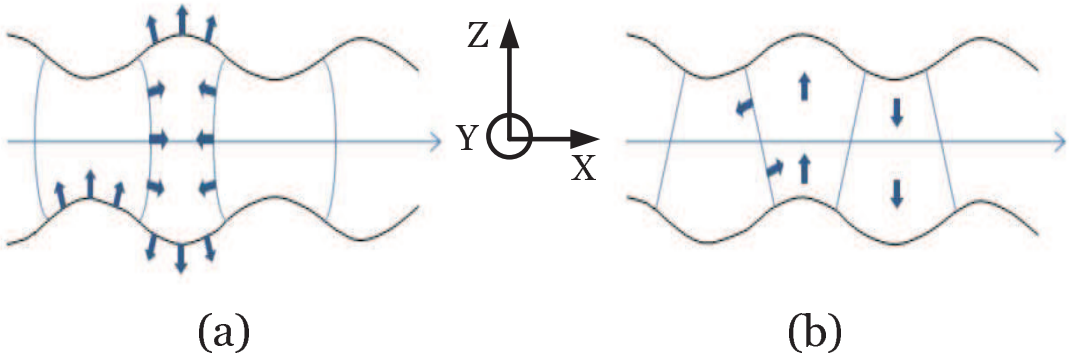

Figure 4.6: Symmetric (a) and asymmetric (b) modes of lamb wave.

LWRs are based on symmetric propagation mode of lamb waves. Although, the configuration of LWRs is similar to FBAR resonators and is composed of a confined piezo-electric material between two electrodes [131] (figure 4.5.b), LWRs present a major advantage compared with BAW resonators. The resonance frequency of BAW resonators depends only to the thickness of the piezo-electric material while LWRs offer two parameters to tune the resonance frequency which are the material width and the material thickness. Hence, the LWR resonance frequency can reach values as small as 40 MHz. In [134] the material thickness of the designed LWR with a resonance frequency equal to 150 MHz is equal to 1.5μm while the width of the material is equal

to $26\mu m$. In spite of this advantage, LWRs are limited in high frequencies because of the limits of the integration technologies [134].

The common disadvantage of piezo-electric resonators is the presence of an anti-resonance in their frequency response caused by the parasite capacitance between the electrodes. Hence, their transfer function does not have a pure band-pass resonator transfer function form. However, compared with classical resonators (Gm-C, Gm-LC, et), b_0 in the numerator of equation 3.14 does not exist. As a result, piezo-electric resonators are open-circuit at DC.

Of all these solutions, LWRs are the only one able to work in the band of interest of the present work with no integration issue.

4.2 Characteristics of LWRs

4.2.1 Electrical model

In general the Butterworth-Van Dyke electrical model (figure 4.7) is used to model a piezo-electric resonator around its fundamental resonance frequency [135]. R_m, C_m and L_m are, respectively, the motional resistance, capacitance and inductance. R_m

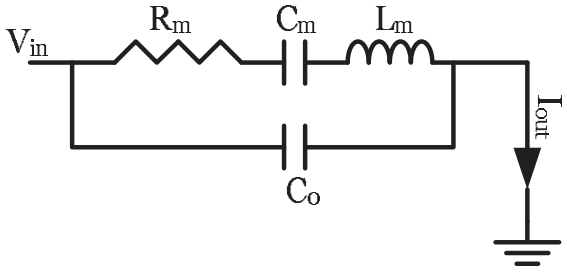

Figure 4.7: Equivalent model of a one-port piezo-electric resonator.

represents the acoustic losses of the resonators and C_0 is the inherent static capacitance between the input and output electrodes. C_0 depends on the electrical permittivity (ϵ) of the acoustic material, the thickness (H) of the resonator and the surface (S) of the electrodes:

$$C_0 = \frac{\epsilon S}{H}. \tag{4.4}$$

The resonance pulsation ($\omega_s = 2\pi f_r$) and the anti-resonance pulsation ($\omega_a = 2\pi f_a$) of piezo-electric resonators depend on the wave guide characteristics of the acoustic material and the shape of the electrodes. The resonator must be modeled through the finite element method to extract ω_r and ω_a. Since the width and the thickness of the material (figure 4.8) must be at least taken into account, a 3-D simulator, like HFSS, is required. Afterward the following relations link ω_r and ω_a to the electrical model parameters:

$$\omega_r = \frac{1}{\sqrt{L_m C_m}}; \quad \omega_a = \sqrt{\frac{C_m + C_0}{L_m C_m C_0}}; \quad Q = \frac{1}{R_m}\sqrt{\frac{L_m}{C_m}}. \tag{4.5}$$

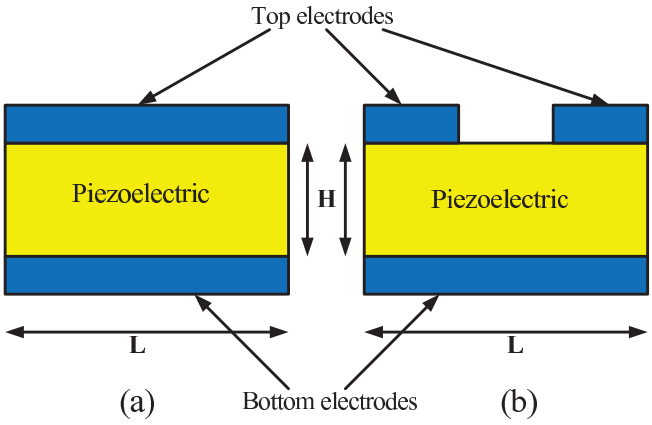

Figure 4.8: Lamb wave resonator working on (a) fundamental (b) third harmonic.

The resonator impedance is given by:

$$Z_{res}(s) = \frac{1}{C_0 s}\frac{s^2 + \frac{R_m}{L_m}s + \frac{1}{L_m C_m}}{s^2 + \frac{R_m}{L_m}s + \frac{C_m + C_0}{L_m C_m C_0}}. \tag{4.6}$$

Also, the approximate transfer function of LWR around the resonance frequency is as follows:

$$H_{res} = \frac{I_{out}}{V_{in}} = \frac{(C_m + C_0)s + R_m C_m C_0 s^2 + C_0 L_m C_m s^3}{1 + R_m C_m s + L_m C_m s^2}. \tag{4.7}$$

Since LWR must be driven in voltage-mode and its output is in current-mode, the LWR transfer function is a trans-inductance function.

The present work is based on the parameters (given in table 4.1) of an LWR designed in [131]. The finite element model is done with ATILA software [136]. This design is

chosen because the resonance frequency of the resonator corresponds to the frequency band of interest in this work. Moreover, its Q-factor corresponds to the requirements of classical wide-band $\Sigma\Delta$ modulators.

Table 4.1: Employed LWR characteristics [131]

f_r	R_m	C_m	L_m	C_0	Q
100 MHz	100 Ω	212 fF	12 nH	1.8 pF	75

4.2.2 Anti-resonance

Due to the parasitic capacitance (C_0), the LWR does not have an ideal second-order resonator transfer function (equation 4.7). The frequency response of the considered LWR (table 4.1) is represented in figure 4.9.

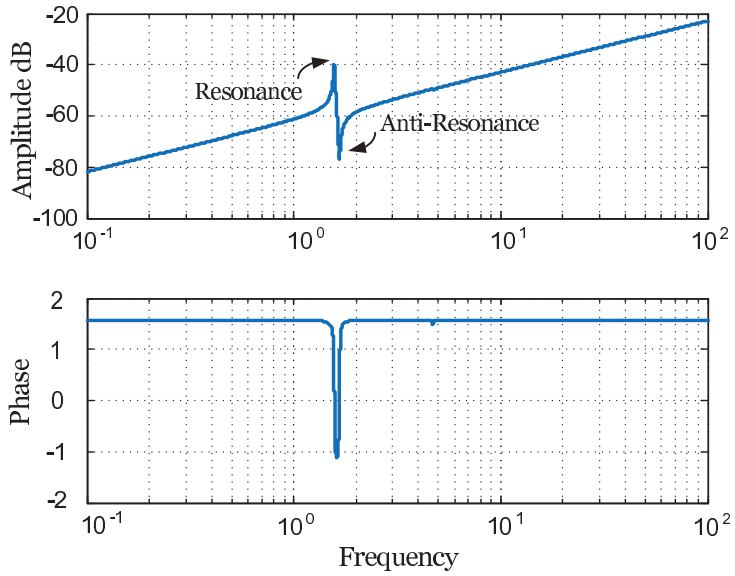

Figure 4.9: Frequency response of the LWR corresponding to table 4.1.

The global filter $G(s)$ transfer functions of an MSCL 6^{th}-order $\Sigma\Delta$ modulator employing a pure resonator transfer function and that of the considered LWR are compared in figure 4.10. Visibly, the parasitic capacitance deteriorates the modulus of the global filter close to the central frequency and, predictably, the modulator performance.

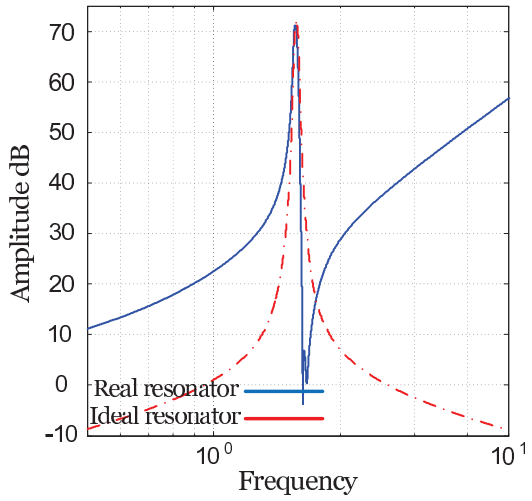

Figure 4.10: Comparison the global filter transfer function of a 6^{th}-order $\Sigma\Delta$ modulator employing an ideal band-pass resonator and a practical LWR.

A solution to eliminate the anti-resonance frequency is represented in figure 4.11. A compensation capacitance (C_c) is put in parallel with the parasitic capacitance of the resonator. The idea consists in driving the resonator and the compensation capacitance in differential-mode.

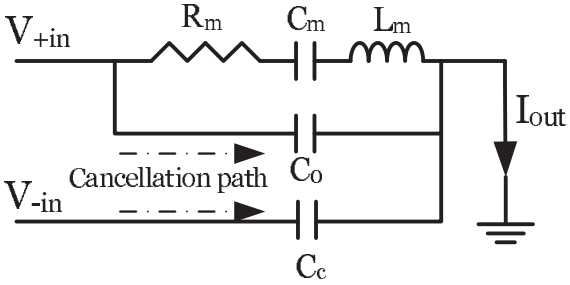

Figure 4.11: Principle of anti-resonance cancellation.

As a result, C_c effectively acts as a negative capacitance. The transfer function of the compensated resonator (figure 4.11) is given by:

$$H_{res} = \frac{I_{out}}{V_{in}} = \frac{C_m s + (C_0 - C_c)(L_m C_m s^3 + R_m C_m^2 + s)}{1 + R_m C_m s + L_m C_m s^2}. \tag{4.8}$$

The anti-resonance is eliminated if C_c is equal to C_0 and the resulting transfer function is given by:

$$H_{res} = \frac{I_{out}}{V_{in}} = \frac{C_m s}{1 + R_m C_m s + L_m C_m s^2}. \tag{4.9}$$

The frequency responses of the non-compensated resonator and that of the fully-compensated resonator corresponding to table 4.1 are compared in figure 4.12.

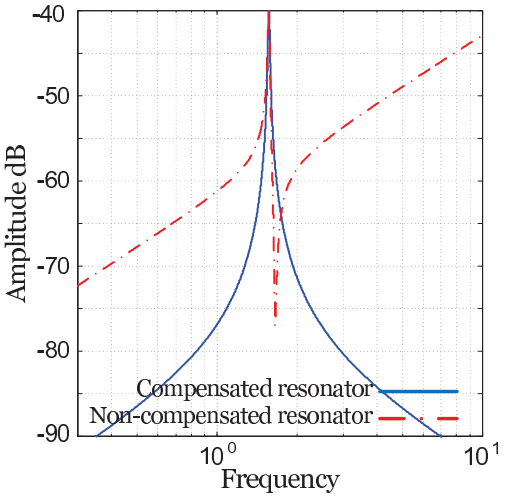

Figure 4.12: Compensated resonator and non-compenated resonator transfer functions.

4.2.3 Quality factor

The Q-factor of a piezo-electric resonator depends mostly on two factors:

1. Acoustic losses which are the result of dissipation in the piezo-electric material, the membrane and the electrodes.

2. Electrical losses which are related to the resistivity of the electrodes.

Nowadays, the trend in the design of piezo-electric resonators is to diminish both of loss mechanisms in order to increase the Q-factor. Table 4.2 presents the state of the art of LWR design. These LWRs achieve high Q-factors (above 1000) while the required Q-factor in the present work is around 100.

One may decrease the Q-factor by increasing the electrical losses, in other words by adding an electrical resistance in series with the motional resistance (R_m). This is not a convenient solution when considering the difference between the effects of acoustic

Table 4.2: State of the art of LWRs

Structure	Lamb [134]	Lamb IDT [137]	Lamb [138]	Flexion [139]	Contour [140]
f_r	$92MHz$	$570MHz$	$885MHz$	$210MHz$	$230MHz$
Q	2000	880	3000	3000	4300

losses and those of electrical losses on the Q-factor. As can be seen from figure 4.13, increasing electrical losses results in decreasing the Q-factor but also in decreasing the magnitude at the resonance frequency. Hence, a larger amplification is required to compensate for the insertion loss which complicates the design of the electronic control circuits. On the other side, increasing acoustic losses results only in decreasing the Q-factor with no magnitude changes at the resonance frequency.

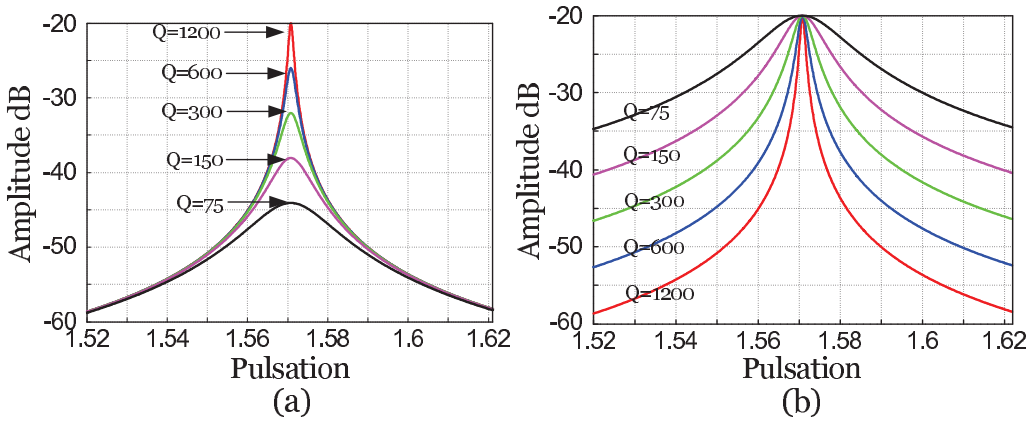

Figure 4.13: Influence of electrical (a) and acoustic (b) losses on the Q-factor.

State of the art of LWRs is low dissipation resonators designed to obtain a large Q-factor. This is the main drawback of using LWRs in wide-band $\Sigma\Delta$ modulators. Although our research indicates that the design of a convenient LWR is possible by using high-loss piezo-electric materials and new structures, this is an independent field of research which is beyond the scope of this work.

4.2.4 Harmonic content

The harmonic content of resonators are an issue in electronic design. Because of the presence of a sampler in the ΣΔ modulator loop, high-order harmonics may be folded back into the frequency band of interest. Usually a low-pass filter is used to reduce the magnitude of the resonator harmonics. Such a solution introduce a phase delay in the ΣΔ modulator loop. Moreover, the electronic control circuits are designed in differential-mode to eliminate the even harmonics. However, the influence of reduced interferer on the modulator performance must be studied.

For this aim, an electrical equivalent model of the harmonic content is required. As a result the harmonics resonance, anti-resonance and parasitic capacitance must be extracted through simulation. Since the harmonics properties of the considered LWR is unknown for us, an approximate model represented in figure 4.14 is used to model the third and fifth harmonics of LWR. The even harmonics are eliminated in a differential-mode design and the magnitudes of higher-order harmonics are generally small.

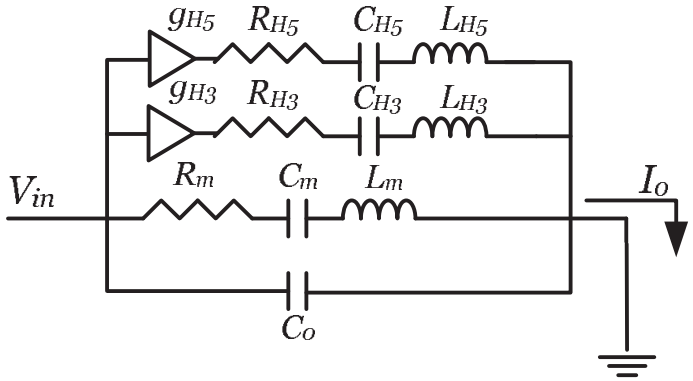

Figure 4.14: Approximate electrical model of LWR considering the third and fifth harmonics.

For the sake of simplicity, the acoustic losses at harmonics frequencies are considered equal to those of the fundamental resonance frequency. Then $R_m = R_{H3} = R_{H5}$. Also, the parasitic capacitances at harmonics are neglected. Since the third harmonic pulsation (ω_{H3}) is equal to $3\omega_r$ and that of the fifth harmonic is equal to $5\omega_r$, C_{H3}, L_{H3}, C_{H5} and $_{H3}$ can be calculated as follows:

$$\begin{cases} C_{H3} = \frac{1}{3*Q*R_m*\omega_r}, & L_{H3} = \frac{Q*R_m}{3*\omega_r} \\ C_{H5} = \frac{1}{5*Q*R_m*\omega_r}, & L_{H5} = \frac{Q*R_m}{5*\omega_r}. \end{cases} \tag{4.10}$$

Finally, g_{H3} and g_{H5} determine the magnitude of the frequency response of the resonator at harmonic frequencies. They depend on the waveguide properties of the LWR and can be extracted from simulation. In the present work, they are set by hand to determine the stability limits of ΣΔ modulators as explained in the following chapter. The resulting frequency response for typical values of g_{H3} and g_{H5} is shown in figure 4.15.

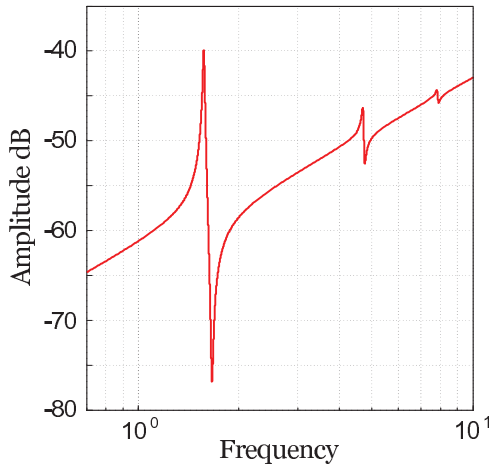

Figure 4.15: Frequency response of the electrical model of figure 4.14

4.3 Resonator circuit

The performance of high-order modulators is sensitive to the resonator performance. Therefore, a robust electronic control circuit is required to ensure the performance of the LWR. Indeed, the LWR performance is guaranteed by adequate input and output impedances of the electronic control circuit and anti-resonance cancellation. Moreover, the resonator gain must be provided by the control circuit since LWRs are passive devices. Figure 4.16 presents the required electronic control circuit to overcome the issues where x is the representative of LWR.

The structure includes two buffer stages. Note that a ΣΔ modulator contains several nodes where the output of different components must be added together. Hence, the

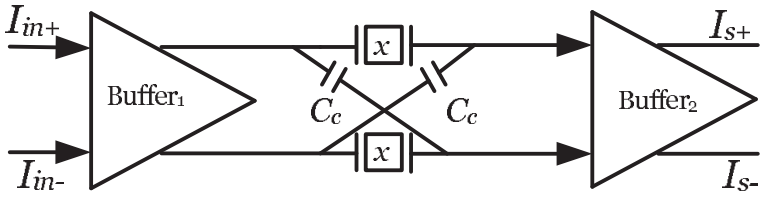

Figure 4.16: Electronic control circuit of the LWR.

modulator usually works in current-mode because the add function can be done easily by mixing the signal paths with no need of extra enhancement. As a result, the input of the resonator circuit is in current-mode while LWRs must be driven in voltage-mode. Therefore, the first buffer is a trans-impedance circuit converting the input current to a drive voltage. It also provides the resonator gain and a low output impedance. The output of the LWR is in current-mode so the second buffer is a current-to-current converter providing a low input impedance. The equivalent model of the positive path of the proposed structure is shown in figure 4.17.

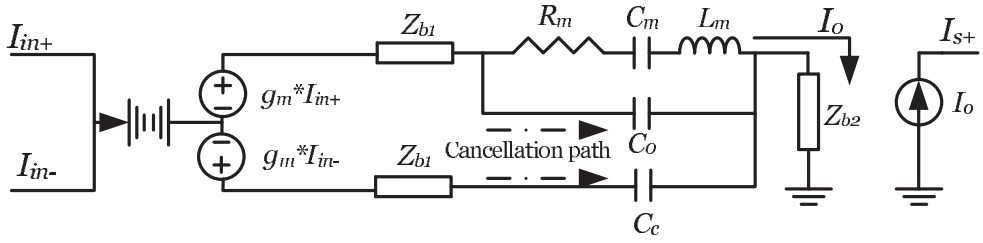

Figure 4.17: Equivalent model of the positive path of the electronic control circuit.

g_m is the trans-impedance gain of the first buffer given by:

$$g_m = \frac{g_0}{1 + \frac{s}{\omega_b}}, \tag{4.11}$$

where g_0 is the DC trans-impedance gain and ω_b is the first pole frequency. The other poles frequency, including the second buffer ones, are not considered because they are not critical. Although the first buffer output impedance (Z_{b1}) and the second buffer input impedance (Z_{b2}) must be theoretically null, this is not possible in practice. Then, they must be sufficiently small compared with the resonator impedance at the resonance frequency. The transfer function of the proposed topology is then as follows:

$$H_{res} = \frac{I_s}{I_{in}} = \left(\left((Z_{b1} + Z_{lwr})^{-1} - \left(Z_{b1} + \frac{1}{C_c s} \right)^{-1} \right)^{-1} + Z_{b2} \right) \left(\frac{g_0}{1 + \frac{s}{\omega_b}} \right), \quad (4.12)$$

where H_{lwr} is given by:

$$Z_{lwr} = \left(\frac{1}{R_m + L_m s + \frac{1}{C_m s}} + \frac{g_{H3}}{R_{H3} + L_{H3} s + \frac{1}{C_{H3} s}} + \frac{g_{H5}}{R_{H5} + L_{H5} s + \frac{1}{C_{H5} s}} + \frac{1}{C_0 s} \right)^{-1}. \quad (4.13)$$

Assuming that the amplitude of the harmonics are negligible ($g_{H3} = g_{H5} \cong 0$), the buffers are well designed ($g_0 >> \frac{1}{L_m C_m}$, $Z_{b1} \cong Z_{b2} << Z_{res}$, $\omega_b >> 2 * \pi f_c$) and $C_c = C_0$, the transfer function of figure 4.16 can be expressed by:

$$H_{res} = \frac{I_s}{I_{in}} = \frac{g_0 C_m s}{1 + R_m C_m s + L_m C_m s^2}. \quad (4.14)$$

Although equation 4.14 is not achievable in practice, it is useful to synthesize the modulator global filter transfer function. Afterward, equation 4.12 is used to study the influence of analog imperfections of the resonator on the modulator performance.

4.4 Conclusion

In order to find the most suitable kind of resonators, three sorts of resonators (classical resonators, micro-mechanical resonators and piezo-electric resonators) were studied. Although the classical resonators are the most compatible with integration technologies, they are not able to provide large Q-factors. Moreover, employing Q-enhancement circuits deteriorates the linearity of resonators.

Micro-mechanical resonators were also considered. High Q-factor is one of major characteristics of MEMS. However, integration issues caused by the encapsulation and their high bias voltage prevents the use of MEMS.

Finally, the resonators based on the piezo-electric material have been studied. They are categorized in three common types (SAW, BAW and LWR resonators). Although they are able to attain large Q-factors, they are not all convenient for the aim of the present work. The main disadvantage of SAW resonators is the integration difficulties. BAW resonators can be integrated but their resonance frequency can not be smaller

than 800 MHz. LWRs make it possible to work with a resonance frequency between 40 MHz and 900 MHz. Therefore, it seems that LWRs are good candidates, compared with other kinds of piezo-electric resonators, for being used in $\Sigma\Delta$ modulator applications.

An approximate electrical model of LWRs based on Butterworth-Van Dyke electrical model was presented to model the LWR close to its fundamental resonance frequency. This model makes it possible to take into account the existence of the third and fifth harmonics of the LWR.

An electronic control circuit has been also proposed to overcome the main issues of LWRs (anti-resonance cancellation and low impedance connections). The transfer function of the proposed circuit, including major non-idealities, has been calculated in order to study the influence of analog imperfections on the modulator performance.

5

High-Order Single-Stage Delta-Sigma Modulators

If the loop delay is between $1T_s$ and $2T_s$ and $f_c \neq 0.25f_s$ the topology of figure 3.14 is not an exact implementation of equation 2.13 but an approximate one. Because of the absence of $T_1(z)$, the resulting NTF does not correspond to that of the original DT modulator. Indeed, compared with the exact implementation of equation 2.13 (figure 2.17), the modulus of the equivalent DT loop filter is maintained close to the modulator central frequency (figure 5.1.a) while the positions of the NTF poles are modified (figure 5.1.b).

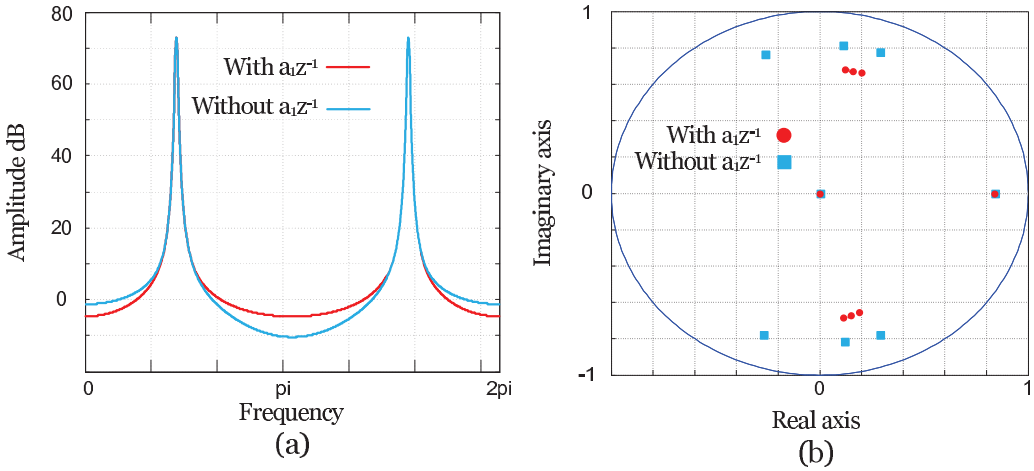

Figure 5.1: Influence of $T_1(z) = a_1 z^{-1}$ on the modulus of the DT equivalent of the global filter (a) and the position of the NTF poles (b) for $f_c = 0.22f_s$.

Therefore, as it is shown in the simulation results of the proposed topology (figure 3.16), the stability margin is reduced when moving toward the band edges ($0.2f_s$ and $0.3f_s$) and the resolution is not affected. In practice, this reduced stability margin is not satisfying in terms of analog imperfections. Indeed, the modulator becomes almost certainly instable by analog imperfections especially at the band edges ($0.2f_s$ and $0.3f_s$). Therefore, a proper design methodology is required. The objective is to increase the stability margin as well as maintaining the resolution across the frequency band of interest ($0.2f_s < f_c < 0.3f_s$) by modifying the global filter transfer function.

First of all, a convenient topology to synthesize the global filter transfer function ($G(s)$) is needed. This topology must provide an adequate control of the position of the NTF poles by simple means. The topologies proposed in recent studies are based in general on multi-feedback techniques [141], [63]. The control of the NTF poles is done by separately tuning the pulses of two DACs in the feedback loop. Extra feedbacks are also needed to compensate for excess loop delay [142]. Since high-order modulators are sensitive to DAC linearity, this is not a convenient solution to control the position of the NTF poles. Assuming that e_{DAC} is the introduced error by the DAC to its analog output signal ($e_{DAC} = DAC_{\text{output}} - \Delta DAC_{\text{input}}$, where Δ represents the gain of the DAC), in [143] it is shown that the following relation must be respected to ensure the performance of the modulator:

$$\frac{e_{rms}}{DO_{max}} < \frac{1}{\sqrt{2} * 2^{\text{ENOB}+1}}, \tag{5.1}$$

where e_{ems} is the root mean square of e_{DAC} and DO_{max} is the full-scale input of the DAC. As an instance, to attain a resolution up to 18-bits, the maximum of the introduced error must be less than 2^{-19}. Although this precision is out of reach regardless of the employed technology, DAC linearity is achievable by Dynamic Element Matching (DEM) algorithms [143], [144], [145], [146], [147]. These methods result in increasing the consumption and the size of the circuit. These disadvantages are doubled for multi-feedback techniques.

In this chapter, we propose a new topology based on weighted feedforward techniques to implement the CT global filter transfer function. The main advantages include using only one DAC with a single feedback path and providing the control on the position of the NTF poles with feedforward coefficients. An exact method of synthesis is also proposed to find a proper start-point for the optimization method.

Since CT modulators are sensitive to analog imperfection, a sensitivity study is required to determine the influence of non-idealities on the modulator performance. The sensitivity study is based on the results of the synthesis method and the ideal components are replaced by their simple models, including their major non-idealities, to determine the most troublesome parameters.

The sensitivity study shows that because of the considered non-idealities, the modulator is instable even for $f_c = 0.25 f_s$. Note that the topology of figure 3.14 is exact for $f_c = 0.25 f_s$. Therefore, analog imperfections must be also considered in the optimization method. The flowchart of the proposed optimization method is shown in figure 5.2.

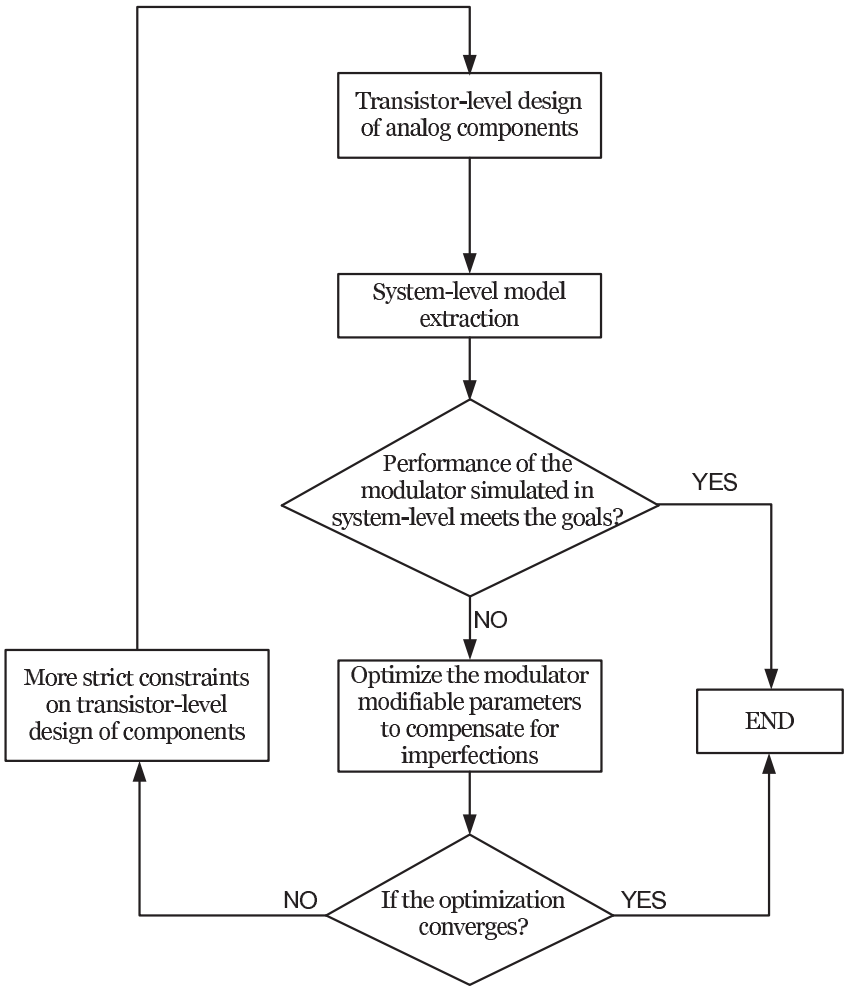

Figure 5.2: Proposed optimization method.

In order to be reliable in practice, the system-level model of the designed analog components in transistor-level in the chosen technology kit must be extracted. The ideal components of the modulator are replaced by the extracted model accounting non-idealities. Afterward, the modifiable parameters of the proposed structure are optimized to recover the modulator performance.
When the optimization does not converge, this means that the deviation of the characteristics of the transistor-level designed components from their nominal values is extremely large. Then, from the sensitivity study, the constraints on the design of the troublesome parameters should become more strict. When the optimization method converges, the performance of the modulator is guaranteed in practice.

Adding new constraint to the optimization method in order to obtain a filtering-STF is not realistic. Some signal paths are added to the proposed topology to be able to modify the STF without changing the global filter.

5.1 Modulator global filter synthesis

5.1.1 Global filter topology

The topology of figure 5.3 is proposed to synthesize the global filter transfer function.

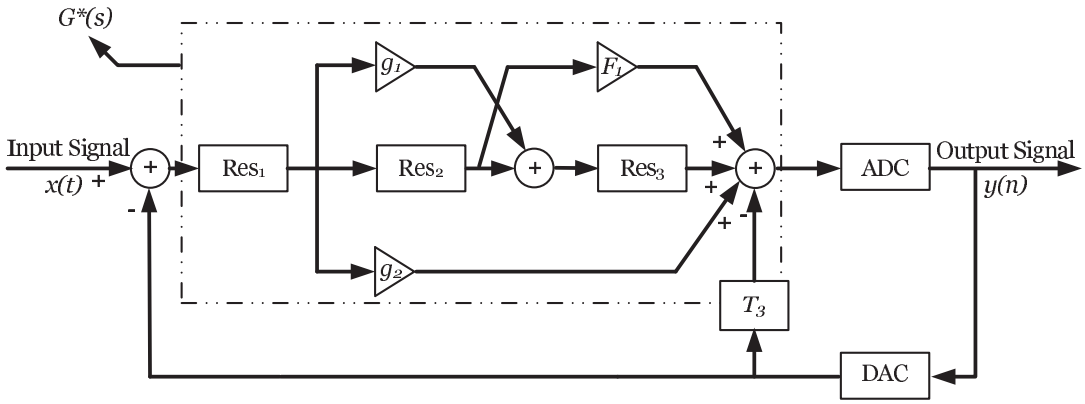

Figure 5.3: The topology proposed to synthesize the global filter transfer function.

Three band-pass resonators are put in series and their transfer functions are given by:

$$H_{Res_i} = \frac{num_i(s)}{den_i(s)} = \frac{b_i s}{a_{i1} + a_{i2} s + s^2} = \frac{b_i s}{\omega_{c_i}^2 + \frac{\omega_{c_i}}{Q_i} s + s^2}. \tag{5.2}$$

The global filter transfer function ($G^*(s)$) of the proposed topology is given by:

$$G^*(s) = H_{Res_1} \left[(F_1 + H_{Res_3}) H_{Res_2} + g_2 + g_1 H_{Res_3} \right]. \tag{5.3}$$

Substituting H_{Res_i} in equation 5.3 by equation 5.2 results in:

$$G^*(s) = \frac{b_1 s}{a_{11} + a_{12} s + s^2} \left[\left(F_1 + \frac{b_3 s}{a_{31} + a_{32} s + s^2} \right) \frac{b_2 s}{a_{21} + a_{22} s + s^2} + g_2 + g_1 \frac{b_3 s}{a_{31} + a_{32} s + s^2} \right]. \tag{5.4}$$

$G^*(s)$ can be also represented by :

$$G^*(s) = \frac{c_5 s^5 + c_4 s^4 + c_3 s^3 + c_2 s^2 + c_1 s}{\prod_3^{i=1} den_i(s)}. \tag{5.5}$$

The denominator of $G^*(s)$, determining the modulator resolution, is already set by imposing the resonator resonance frequency and the Q-factor through the explained specifications in chapter II (figure 3.8 and figure 3.9). Considering the form of the numerator of $G^*(s)$ (equation 5.5), synthesizing the modulator global filter transfer function ($G(s)$ calculated through equation 2.13) by $G^*(s)$ meets two major problems.

1. The topology of figure 5.3 provides, only, four independent modifiable parameters useful to fit $G(s)$ by $G^*(s)$. Four degrees of freedom (F_1, g_1, g_2 and b_2) are not sufficient to synthesize a fifth-order polynomial. Note that in the framework of the modulator linear model, the influence of b_1 and b_3 are not independent of other parameters. The proposed solution consists in replacing F_1 by a gain coefficient in parallel with a pure weighted integrator:

$$F_1 = g_3 + g_4 \frac{1}{s}. \tag{5.6}$$

F_1 is not chosen arbitrarily to be replaced. In practice, there is no intention to implement a pure integrator and g_4 is used only to provide a sufficient number of degree of freedom to synthesize $G(s)$. F_1 is the best choice to be replaced because the influence of g_4, at this position, on the modulator performance is negligible

across the frequency band of interest and it can be removed. Also, it does not lead to changes of the form of $G^*(s)$.

2. The global filter transfer function of a 6^{th}-order modulator found through equation 2.13 for a DAC delay equal to $1.5T_s$ at $f_c = 0.25f_s$ is given by:

$$G(s) = \frac{1.66s^5 + 0.55s^4 + 8.28s^3 + 0.65s^2 + 9.9s - 1.77}{s^6 + 0.062s^5 + 7.40s^4 + 0.30s^3 + 18.26s^2 + 0.38s + 15.01}. \tag{5.7}$$

As it is shown, the numerator of $G(s)$ contains a constant term equal to 1.77 (named also s^0 term) whereas the numerator of $G^*(s)$ does not. As a result, the proposed topology is generally not capable of synthesizing $G(s)$ because the global filter transfer functions are not corresponding. In order to achieve a corresponding $G(s)$ to $G^*(s)$, the s^0 term in the numerator of $G(s)$ must be equal to zero. In the next section, it is shown that this term varies with the value of DAC delay and it is possible to make it equal to zero by tuning the DAC delay.

5.1.2 DAC delay management

The variation of the constant term of the numerator of $G(s)$ versus DAC delay is represented in figure 5.4 for different modulator central frequencies in the frequency

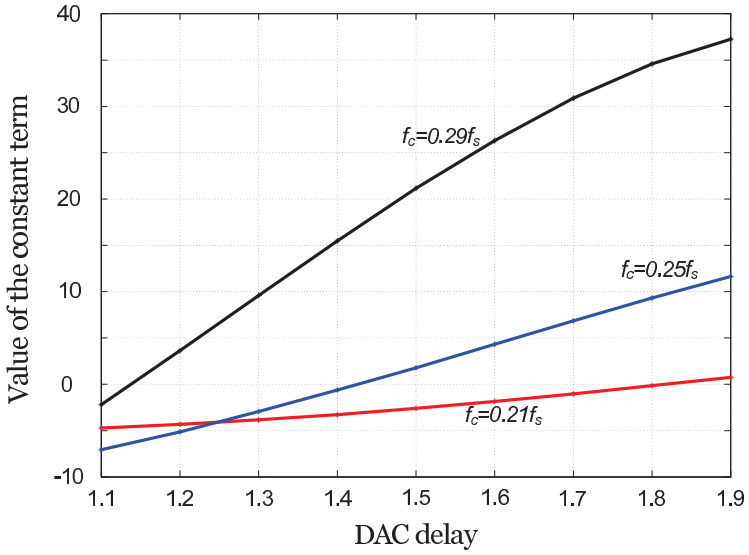

Figure 5.4: Variation of the constant term versus DAC delay for several f_c.

band of interest. Note that, for the sake of simplicity, the DAC delay is defined as the sum of the delays of all components of the modulator loop (including the analog part, the ADC and the DAC).

The results show that across the frequency band of interest, it is always possible to find a value of DAC delay for which the constant term is equal to zero. Moreover, the found DAC delays are between $1T_s$ and $2T_s$. Figure 5.5 presents the values of DAC delay for which the constant term is equal to zero versus the central frequency of the modulator.

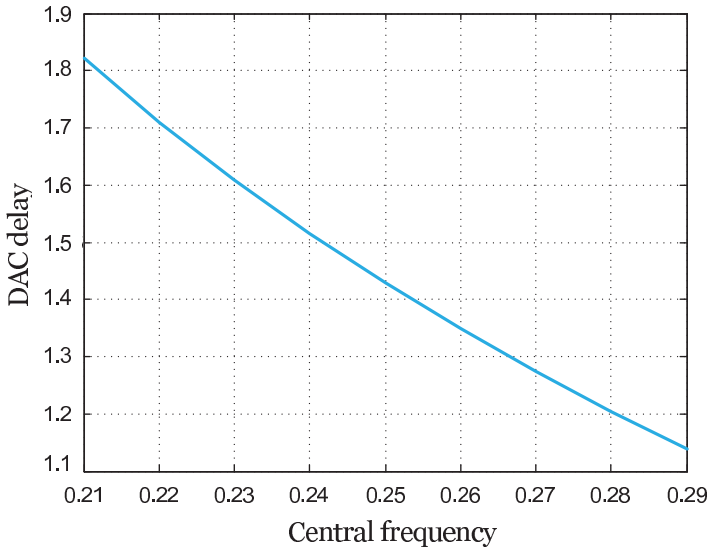

Figure 5.5: DAC delay value canceling out the constant term versus the modulator central frequency.

For example, when $f_c = 0.25f_s$, the DAC delay must be equal to $1.41T_s$ (from figure 5.5) and $G(s)$ becomes as follows (to be compared with equation 5.7):

$$G(s) = \frac{1.62s^5 + 0.83s^4 + 8.21s^3 + 2.00s^2 + 10.01s + 1.61e^{-6}}{s^6 + 0.062s^5 + 7.40s^4 + 0.30s^3 + 18.26s^2 + 0.38s + 15.01}. \tag{5.8}$$

The resulting $G(s)$ is now synthesizable by $G^*(s)$.

5.1.3 Synthesis method

Figure 5.6 is the resulting topology by replacing F_1 with $g_3 + g_4\frac{1}{s}$.
Therefore, the numerator of $G^*(s)$ (equation 5.5) can be expanded as follows:

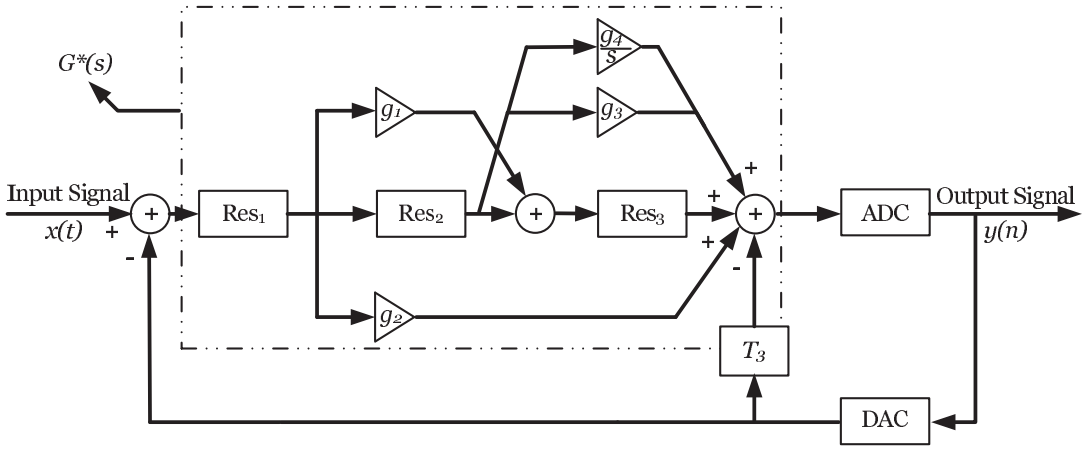

Figure 5.6: Developed topology of figure 5.3.

$$\begin{cases} c_5 = b_1 g_2, \\ c_4 = b_1(g_2 a_{32} + b_2 g_3 + g_1 b_3 + g_2 a_{22}), \\ c_3 = b_1(g_2 a_{31} + g_2 a_{21} + b_2 b_3 + g_1 b_3 a_{22} + g_2 a_{22} a_{32} + b_2 g_3 a_{32} + b_2 g_4), \\ c_2 = b_1(g_2 a_{21} a_{32} + g_2 a_{22} a_{31} + b_2 g_3 a_{31} + g_1 b_3 a_{21} + b_2 g_4 a_{32}), \\ c_1 = b_1(g_2 a_{21} a_{31} + b_2 g_4 a_{31}). \end{cases} \tag{5.9}$$

The numerator ($N_{G(s)}$) and the denominator ($D_{G(s)}$) of $G(s)$ must be, respectively, equated to the numerator ($N_{G^*(s)}$) and the denominator ($D_{G^*(s)}$) of $G^*(s)$. This results in a non-linear system of equations given by:

$$\begin{cases} \sum_{j=1}^{m} D_{G(s)_m} s^m = \sum_{j=1}^{m} D_{G^*(s)_m} s^m \quad \forall s \\ \sum_{i=1}^{n} N_{G(s)_n} s^n = \sum_{i=1}^{n} N_{G^*(s)_n} s^n \quad \forall s \end{cases} \tag{5.10}$$

Newton's method is employed to find the vector of unknown parameters: $[b_2, g_1, g_2, g_3, g_4]$. In this step, b_1 and b_3 are chosen arbitrarily and their values are, respectively, equal to -1 and 0.2. Table 5.1 is the results of Newton's method for different central frequencies. The values of T_3 are also presented which are the results of equation 2.13.

Table 5.1: Synthesized parameters for different modulator central frequencies

Central frequency	$0.21f_s$	$0.23f_s$	$0.25f_s$	$0.27f_s$	$0.29f_s$
b_2	0.6860	0.7004	0.7158	0.7319	0.7489
g_1	1.1028	0.9011	0.6813	0.4340	0.1482
g_2	1.7123	1.6592	1.6211	1.5952	1.5796
g_3	0.7976	0.8372	0.8837	0.9383	1.0032
g_4	0.0291	0.0424	0.0586	0.0784	0.1029
T_3	−0.9548	−0.7702	−0.5825	−0.3949	−0.2102

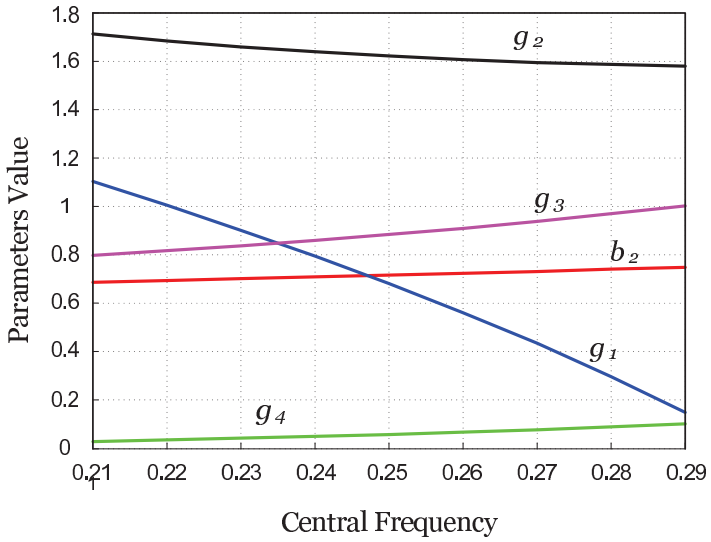

Figure 5.7: Evolution of unknown parameters versus the modulator central frequency.

From figure 5.7, the value of g_4 is negligible across the frequency band of interest and this term can be removed. The final structure is shown in figure 5.8. The performance (modulus margin and bit resolution) of the structure of figure 5.6 is compared with that of the approximate structure of figure 5.8 to show the influence of g_4. The resolution of the modulator is not affected (figure 5.9.b) since it is in relation with the position of the poles of the global filter. On the other side, the stability margin is slightly affected for modulator central frequencies close to $0.3f_s$ (figure 5.9.a) because g_4 becomes a larger value.

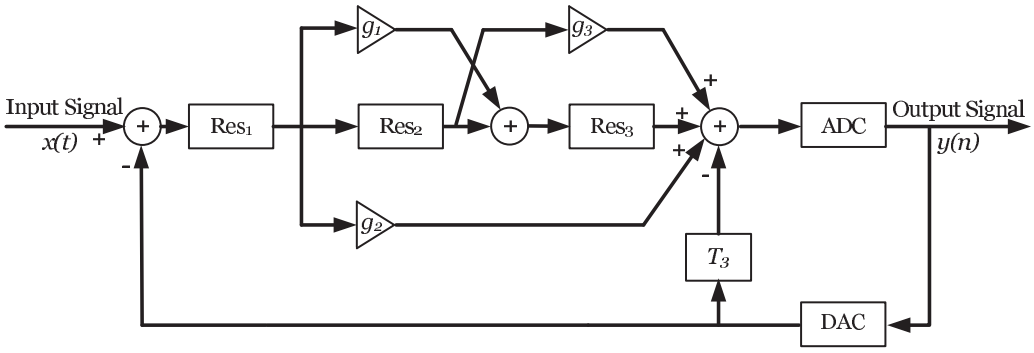

Figure 5.8: Final topology of the modulator.

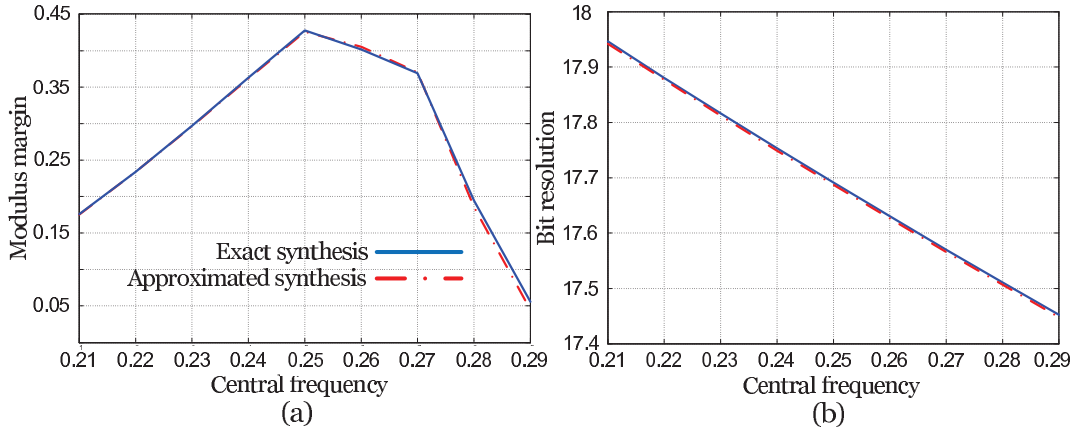

Figure 5.9: Comparison of the performance of the topology of figure 5.6 with the topology of figure 5.8.

5.2 Analog imperfections

Analog imperfections (or non-idealities) are the deviation of the characteristics of the practical component from those of the ideal component. Analog imperfections are inevitable and depend on the manufacturing process (like the position of chip on the wafer) and the characteristics of the chosen technology kit.

A sensitivity study is required to know the influence of different non-idealities on the modulator performance and recognize those with the largest influence. For this aim, major non-idealities of each component are modeled by their simple models. For example, equation 4.12 is used for modeling the imperfections of the resonator control circuit shown in figure 4.17 (the compensation capacitance mismatch, the buffers cut-off

frequencies and the input and the output impedances of the buffers). The sensitivity study is done for $f_c = 0.25 f_s$. In each part of this study, only one parameter is taken into account while the others are considered as ideal. Finally, the modulator is simulated with whole the non-idealities.

5.2.1 Compensation capacitance

In practice, there always exists a mismatch between the compensation capacitance (C_c) and the resonator parasitic capacitance (C_0) (figure 4.11). As a result, the value of the parasitic term in the numerator of equation 4.8 ($(C_0 - C_c)(L_m C_m s^3 + R_m C_m^2 + s)$) is not equal to zero. Figure 5.10 shows the influence of C_c mismatch on the resonator performance for different percentage of error. For a mismatch less than 15% the parasitic term effectively acts as a high-pass filter and for mismatches larger than 15% the anti-resonance frequency re-appears.

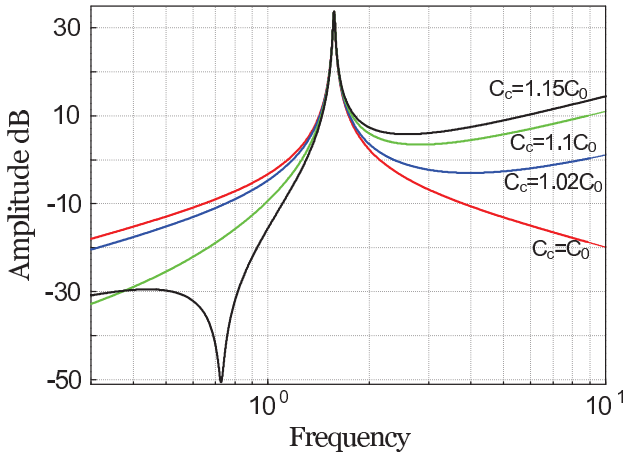

Figure 5.10: Influence of the mismatch between C_c and C_0 on the frequency response of th resonator for different values of error.

The influence of C_c mismatch on the stability margin, the global filter transfer function ($G(s)$) and the position of the NTF poles is shown in figure 5.11.

As it is shown, the modulator becomes instable for a mismatch larger than 2.5%. Since the stability of the modulator is highly sensitive to this parameters, extra solutions must be considered to compensate for this imperfection. On the other side, the resolution of

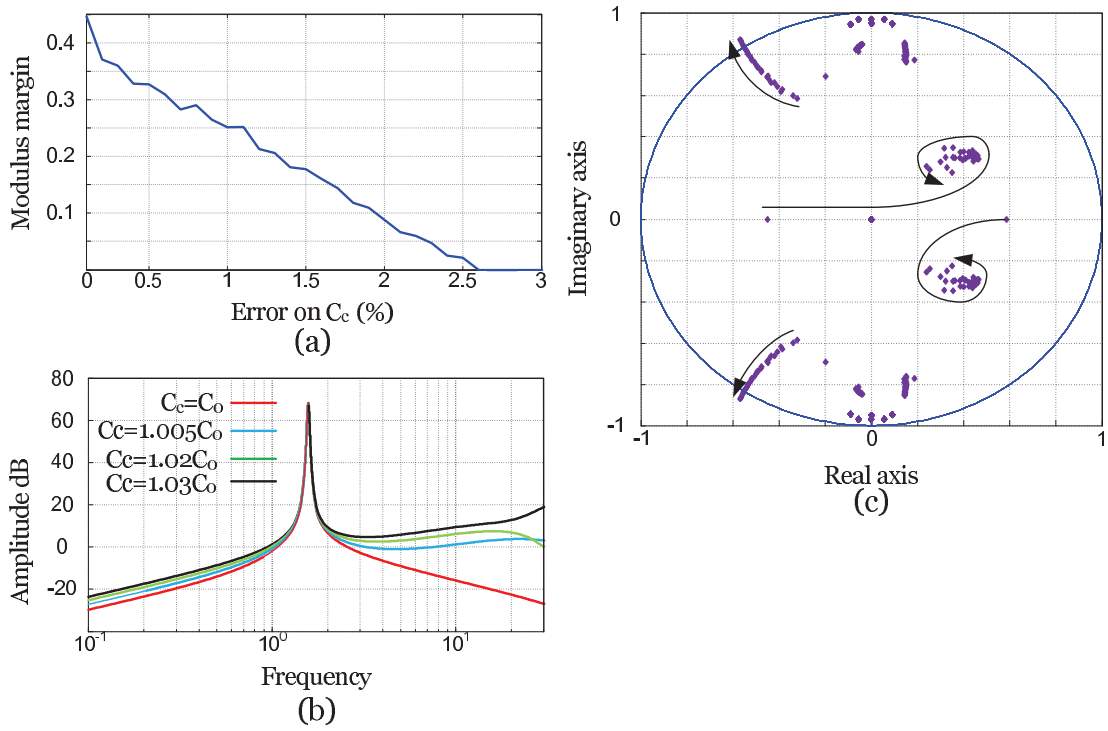

Figure 5.11: Influence of mismatch between C_c and C_0 on the modulus margin (a), the global filter transfer function ($G(s)$) (b) and the position of the NTF poles (c).

the modulator is not affected as long as the modulator stability is maintained because the modulus of $G(s)$ is not deteriorated close to the modulator central frequency.

5.2.2 Buffers cut-off frequency

Figure 5.12 presents the frequency response of the resonator for different value of C_c when the buffer cut-off frequency is infinite ($\omega_b = \infty$) and when the buffer has a pole at $4\omega_c$, where $\omega_c = 2\pi f_c$. Although, theoretically, the cut-off frequency of the buffers should be far away from the operating frequency, it seems from figure 5.12 that the buffer cut-off frequency and the compensation capacitance mismatch act in opposition and they can mitigate with each other to decrease the out-of-band response with no need for additional components. Note that this is correct when the mismatch is less than 15% and results only in a high-pass behavior. For a mismatch larger than 15% the anti-resonance reappears and the cut-off frequency of the buffers is useless.

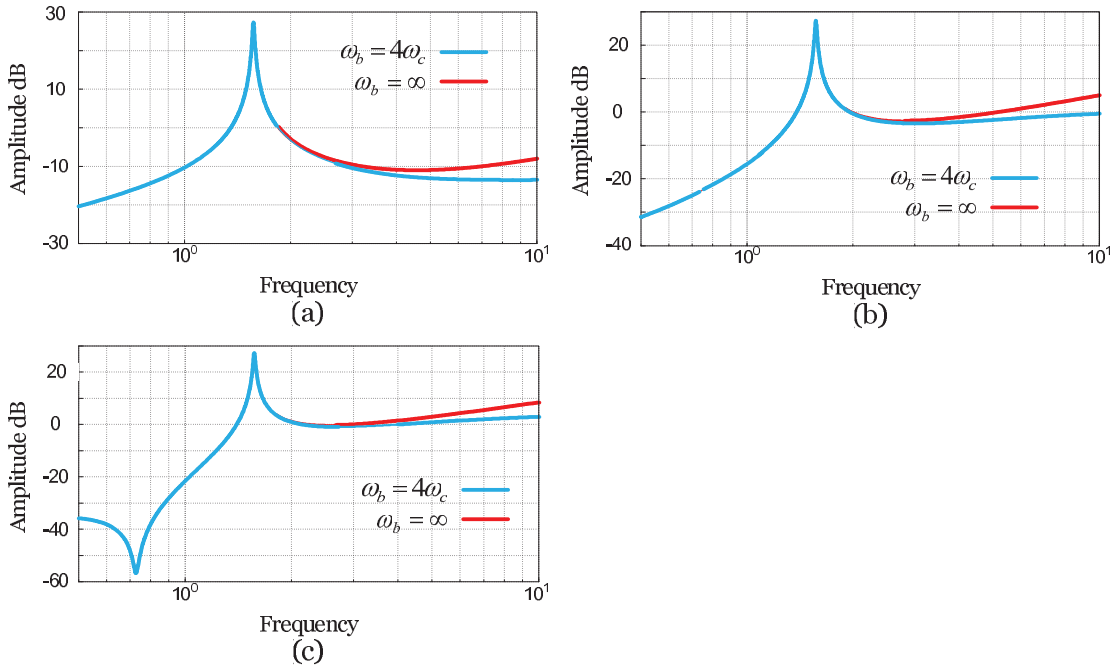

Figure 5.12: Frequency response of the resonator for $C_c = 1.02C_0$ (a), $C_c = 1.10C_0$ (b) and $C_c = 1.15C_0$ (c) when the buffers are ideal ($\omega_b = \infty$) and when they have a pole at $\omega_b = 4\omega_c$

5.2.3 Input and output impedances of the buffers

The output impedance of buffer$_1$ (z_{b1}) and the input impedance of buffer$_2$ (z_{b2}) are in series with the impedance of the LWR (figure 4.16). Assuming that z_{b1} and z_{b2} have an ohmic behavior close to the operating frequency and C_0 is correctly compensated, the Q-factor of the loaded resonator is given by:

$$Q = \frac{1}{z_{b1} + R_m + z_{b2}} \sqrt{\frac{L_m}{C_m}}. \tag{5.11}$$

Non-zero z_{b1} and z_{b2} result in reducing the Q-factor. Therefore, the gain of the forward path is decreased. The resulting loss of the resolution of the modulator is considerable when z_{b1} and z_{b2} are comparable with R_m. The resonator resonance frequency is also affected by the imaginary part of z_{b1} and z_{b2} when they are large. The influence of an ohmic z_{b1} and z_{b2} on the stability margin, the global filter transfer function ($G(s)$) and the position of the NTF poles is shown in figure 5.15. When

$z_{b1} = z_{b2} = \frac{R_m}{2} = 50\Omega$, the amplitude of the global filter is decreased almost 10 dB. This is equivalent of losing 1-bit of the resolution.

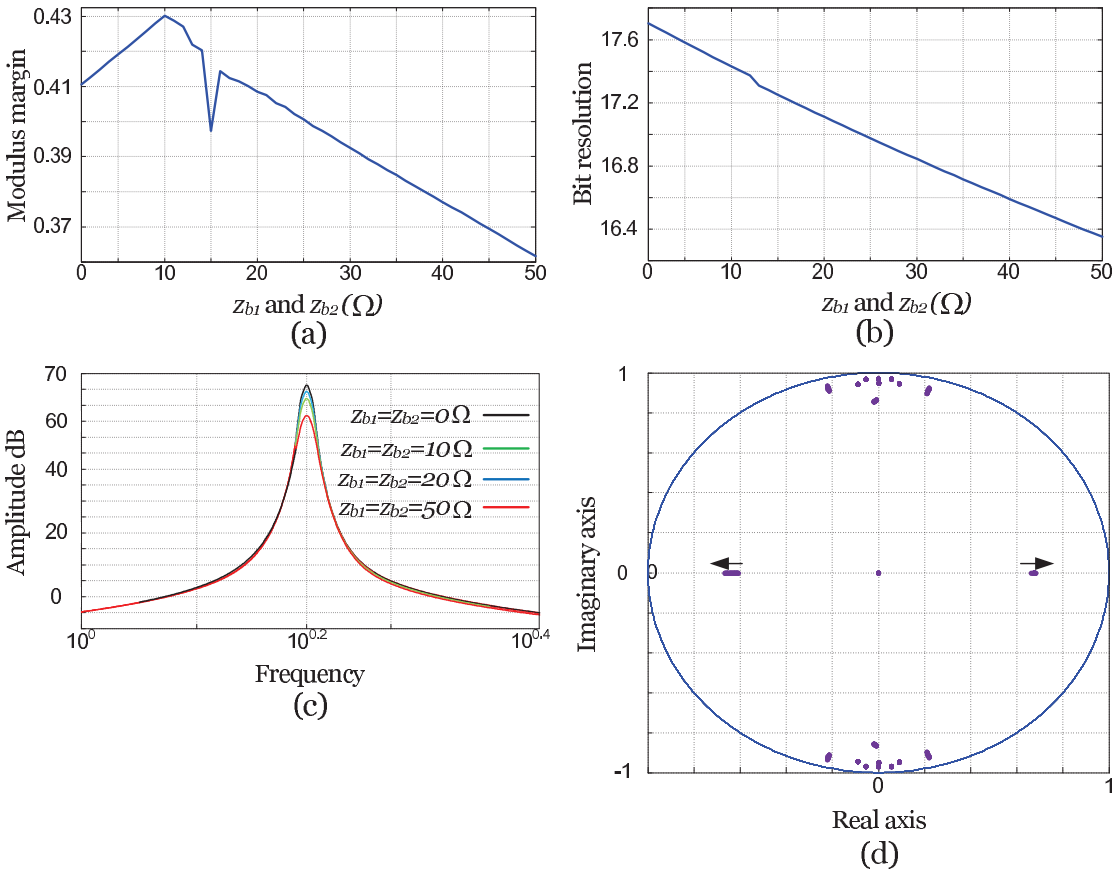

Figure 5.13: Influence of an ohmic z_{b1} and z_{b2} on the modulus margin (a), the resolution (b), the global filter transfer function ($G(s)$) (c) and the position of the NTF poles (d).

5.2.4 Harmonics of LWR

Since the properties of the harmonics of LWRs are unknown in the present work, the amplitude of the harmonics is increased arbitrarily to study the influence of this parameter on the modulator performance. The influence of the amplitude of the third and the fifth harmonics (g_{H3} and g_{H5}) on the stability margin, the global filter transfer function ($G(s)$) and the position of the NTF poles is shown in figure 5.14. It seems that, in the linear framework of the modulator, the harmonics do not have a considerable

influence on the modulator performance. Note that generally g_{H5} is equal to $\frac{1}{3}g_{H3}$ and for a well-designed resonator g_{H3} does not excessed from 0.2.

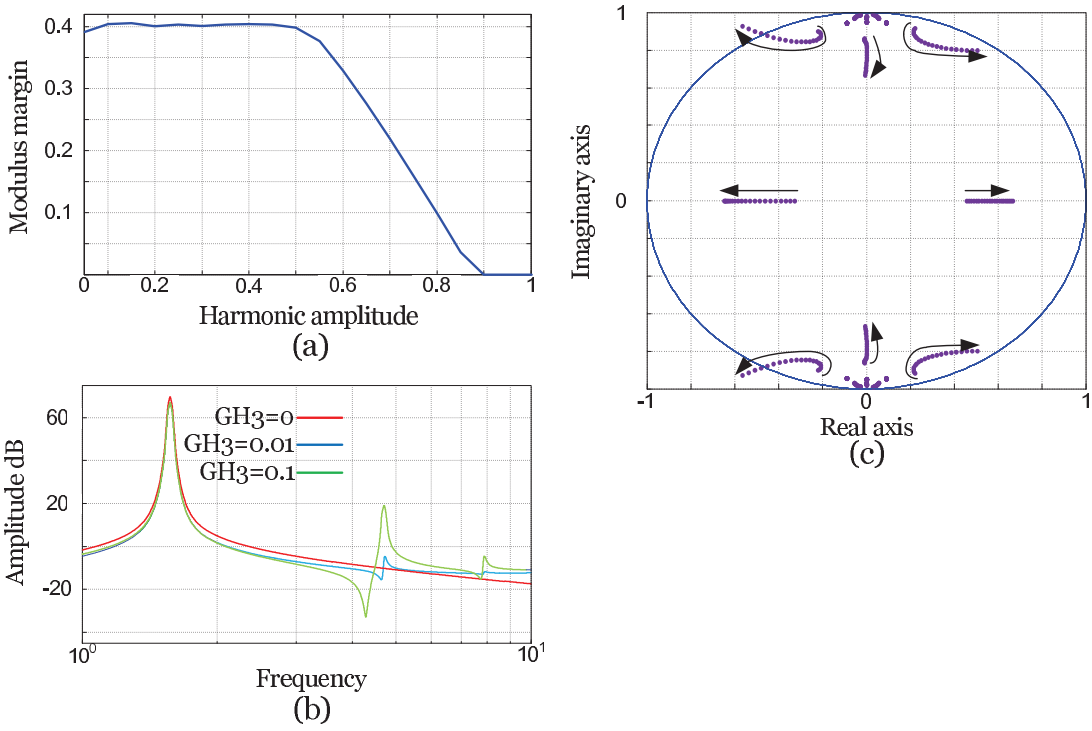

Figure 5.14: Influence of harmonics on the modulus margin (a), the global filter transfer function ($G(s)$) (b) and the position of the NTF poles (c).

5.2.5 Trans-impedance gains

The trans-impedance gains (b_1, b_2 and b_3) determine the gain of the modulator forward path. Their influence on the stability margin, the modulator resolution, the global filter transfer function ($G(s)$) and the position of the NTF poles is shown in figure 5.15. The error percentage is defined by $\frac{b_{i_{\text{practical}}} - b_{i_{\text{nominal}}}}{b_{i_{\text{nominal}}}} * 100$.

Although increasing the gain of the modulator forward path results in increasing $|G(s)|$ and consequently increasing the modulator resolution, the stability margin is decreased because of the characteristics of the looped system. b_1, b_2 and b_3 are useful for performance-adjustment.

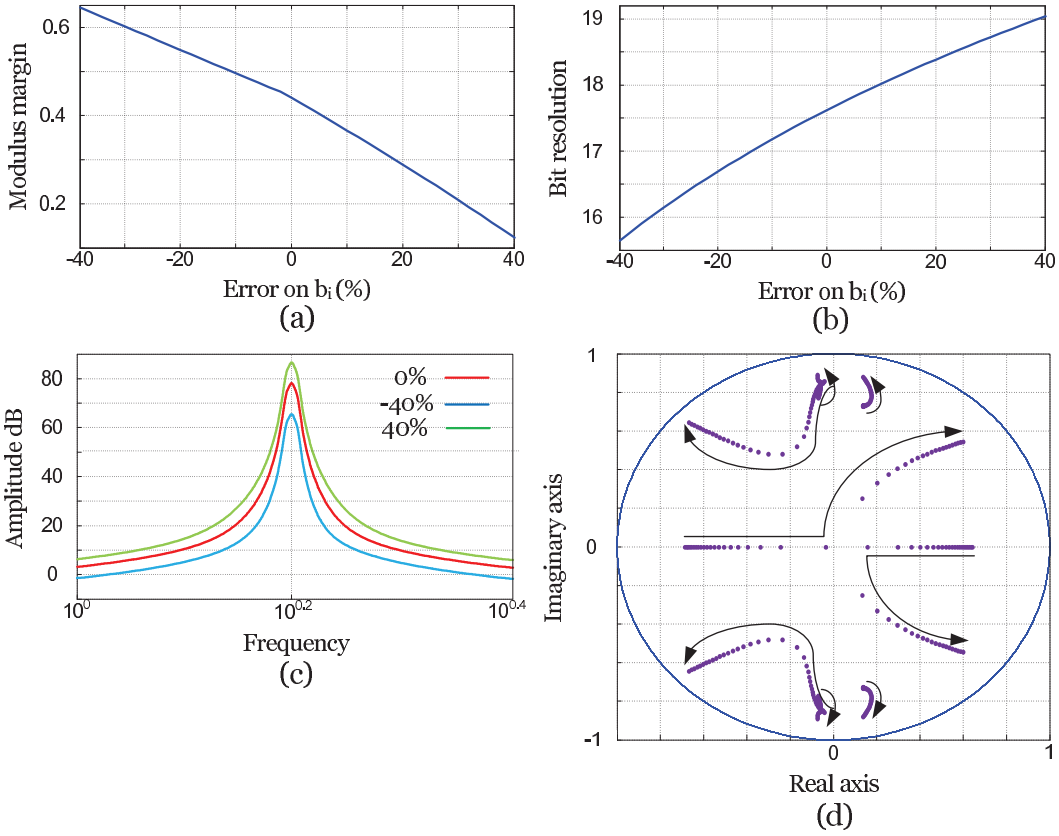

Figure 5.15: Influence of the trans-impedance gains (b_1, b_2 and b_3) on the modulus margin (a), the modulator resolution (b), the global filter transfer function ($G(s)$) (c) and the position of the NTF poles (d).

5.2.6 Feedforward coefficients

The influence of the feedforward coefficients (g_1, g_2 and g_3) on the stability margin, the global filter transfer function ($G(s)$) and the position of the NTF poles is shown in figure 5.16. Note that the error percentage is defined by $\frac{g_{i_{\text{practical}}} - g_{i_{\text{nominal}}}}{g_{i_{\text{nominal}}}} * 100$. Unlike the stability margin, the modulator resolution is not affected. An error in the feedforward coefficients does not lead to change the position of the poles of the global filter. g_1, g_2 and g_3 are useful for performance-adjustment.

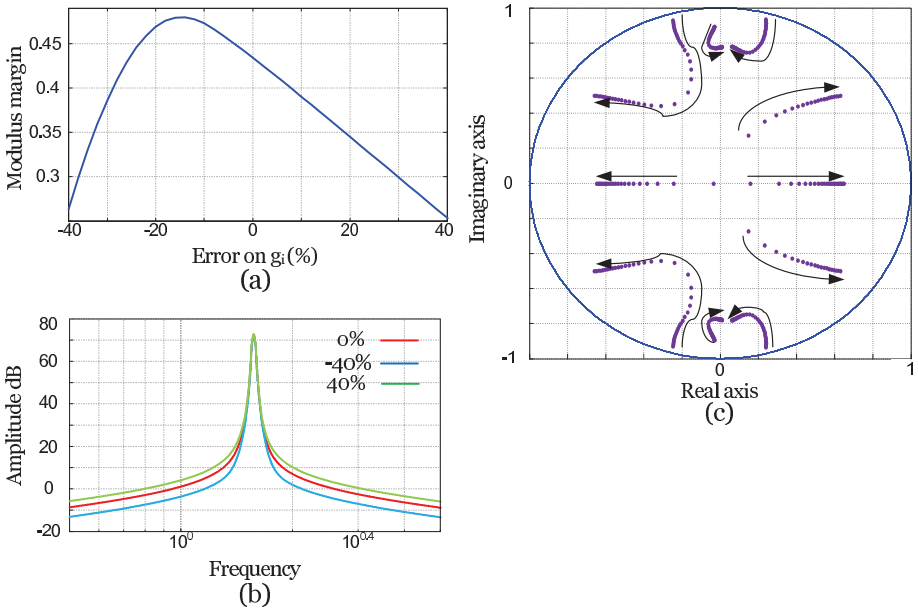

Figure 5.16: Influence of feedforward coefficients (g_1, g_2 and g_3) on the modulus margin (a), the global filter transfer function ($G(s)$) (b) and the position of the NTF poles (c).

5.2.7 Loop delay

CT ΣΔ modulators are very sensitive to the value of the total loop delay (d), in other word, the sum of the delays of analog components, DAC and ADC. Figure 5.17 shows the influence of the loop delay on the stability margin and the position of the NTF poles. As it is shown, the modulator becomes instable for 10% error on the loop delay.

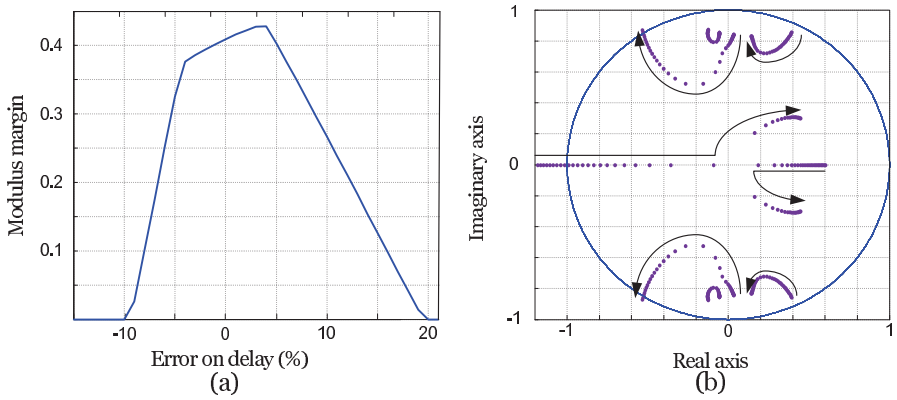

Figure 5.17: Influence of d on modulus margin (a) and position of the NTF poles (b).

Note that the resolution of the modulator is not affected as long as the stability of the modulator is maintained.

5.2.8 All imperfections simulation

The modulator is simulated for several modulator central frequencies in the frequency band of interest with considering the following imperfections:

$$\begin{cases} z_{b1} = z_{b1} = 10\Omega, \\ b_i = (1 + 0.1) * \text{nominal value}, \\ g_i = (1 + 0.1) * \text{nominal value}, \\ C_c = (1 + 0.02)C_0, \\ \omega_b = 4\omega_c, \\ g_{H3} = 0.03, \quad g_{H_5} = 0.01, \\ d = (1 + 0.02) * \text{nominal value}. \end{cases} \tag{5.12}$$

Figure 5.18 shows the resulting modulus margin and resolution versus the modulator central frequency. Although the considered non-idealites are significantly smaller than a practical case, they are sufficient to make the modulator instable for $0.21f_s < f_c < 0.26f_s$ and to significantly reduce the stability margin for $0.26f_s < f_c < 0.29f_s$. Visibly the modulator is highly sensitive to analog imperfections and the design of the proposed structure is not reliable without appropriate solutions to compensate for imperfections.

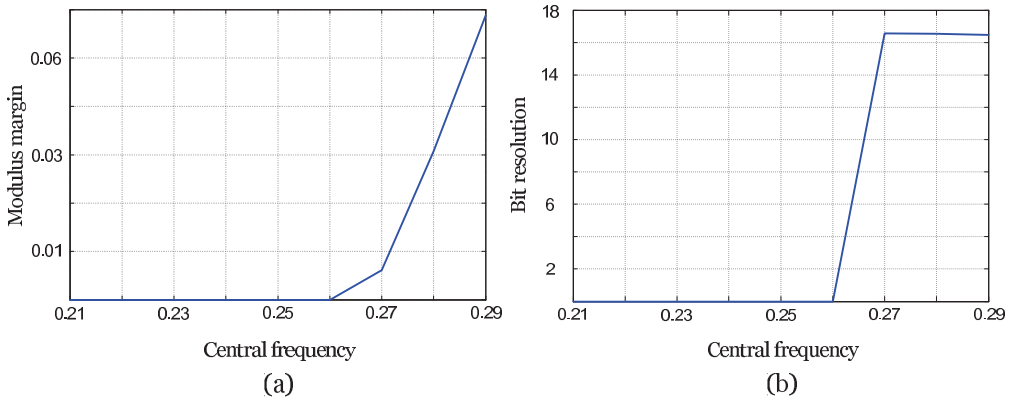

Figure 5.18: Modulus margin (a) and the bit resolution (b) of the proposed topology for various modulator central frequencies accounting analog imperfections given by equation 5.12.

5.3 Optimization method

The sensitivity study shows that the synthesized modulator is highly sensitive to analog parameters. Although sensitivity to analog imperfections is the main characteristic of high-order CT modulators regardless of the topology used to synthesize $G(s)$, the proposed topology provides an adequate control on the position of the NTF poles. This characteristic can be used in order to maintain a good performance in spite of imperfections.

An optimization method to tune the modifiable parameters is required. The objective is achieving the same performance as the original DT modulator by the proposed CT topology at each central frequency. It should be noted that the performance of an ideal DT modulator is independent of f_c (figure 3.16). Hence, meeting the optimization goals should results in a flat performance across the frequency band of interest.

The vector of modifiable parameters used to set the modulator performance (modulus margin and resolution) is given by:

$$\mu = [d,\ T_3,\ g_1,\ g_2,\ g_3,\ b_2]\,. \tag{5.13}$$

Where d corresponds to the value of DAC delay and T_3 corresponds to the loop coefficient (figure 5.8). The optimization criterion (κ) that should be minimized is given by:

$$\kappa = (1 - MM_{CT}) + \lambda_1 \left\| NB_{DT} - NB_{CT} \right\|^2 + \zeta, \tag{5.14}$$

where NB_{DT} is the bit resolution of the original DT modulator, NB_{CT} and MM_{CT} are respectively the bit resolution and the modulus margin of the CT modulator for the specified value of μ. ζ is a smoothing function defined as follows:

$$\zeta = \lambda_2 \sum_i \frac{\partial((1 - MM_{CT}) + \lambda_1 \left\| NB_{DT} - NB_{CT} \right\|^2)}{\partial \mu_i}. \tag{5.15}$$

Although the exact partial derivatives can not be calculated, a finite difference scheme is used to approximate ζ. Without ζ, the optimization criterion (κ) has several local minima and a global minimum. However, the global minimum is not obligatorily a satisfactory answer because of fabrication considerations. The derivative of κ versus some parameters may be large close to some of these minima. In this case, there is a strong

chance for performance degradation because of non-idealities of the implementation of the optimized modifiable parameters. As a result, it is important to study the global behavior of κ around the the minima in function of modifiable parameters and finally eliminate these sharp global or local minima. ζ is introduced to meet this goal. λ_1 and λ_2 are hyper parameters the values of which must be set by the user. For example, if the deviation of the characteristics of the practical components from those of the ideal components is not significant, a large stability margin is not required. Therefore, λ_1 may be increased in order to concentrate on improving the modulator resolution. On the contrary, when a large stability margin is required, λ_2 is increased and λ_1 is diminished. As a result, a resolution loss is accepted (compared with the original DT modulator) to improve the stability margin. The starting value of μ is the value found through the synthesis method. A griding method in association with the "Fmin search" function of MATLAB is used.

In this section, the proposed optimization method is tested by simple models of analog imperfections while system-level models extracted from a transistor-level simulation must be used in order to ensure the performance in practice. The following worst cases are considered:

$$\begin{cases} z_{b1} = z_{b2} = 15\Omega, \\ C_c = (1 + 0.06)C_0, \\ \omega_b = 3\omega_c, \\ GH_3 = 0.06, \quad GH_5 = 0.02, \\ 10\% \ \text{ error on } b_i \text{ and } g_i. \end{cases} \tag{5.16}$$

The modulator is certainly instable for 6% mismatch on C_c (figure 5.11). Beacuase of large considered imperfections, achieving a large modulus margin is prefered rather than improving the modulator resolution. The optimization is done for the following central frequencies: $0.21f_s$, $0.22f_s$, $0.23f_s$, $0.24f_s$, $0.25f_s$, $0.26f_s$, $0.27f_s$, $0.28f_s$ and $0.29f_s$. The optimized values of the modifiable parameters are compared with those of the synthesis method for some central frequencies in table 5.2.

Considering large imperfections results in an optimized loop delay (d) almost equal to $1T_s$ across the frequency band of interest. Then, design of linearization techniques of DAC faces problems. However, in practice, auto-correction methods are used to reduce the non-idealities of the analog components. Therefore, the optimized loop delay is larger than the considered worst case.

Table 5.2: Value of the modifiable parameters before and after optimization

Central frequency	$0.21f_s$	$0.23f_s$	$0.25f_s$	$0.27f_s$	$0.29f_s$
Synthesized b_2	0.6860	0.7004	0.7158	0.7319	0.7489
Optimized b_2	0.4780	0.6099	0.2821	0.3007	0.3189
Synthesized g_1	1.1028	0.9011	0.6813	0.4340	0.1482
Optimized g_1	0.7537	0.7389	1.2408	0.4968	0.1754
Synthesized g_2	1.7123	1.6592	1.6211	1.5952	1.5796
Optimized g_2	2.1648	2.0957	1.4327	1.4374	1.4354
Synthesized g_3	0.7976	0.8372	0.8837	0.9383	1.0032
Optimized g_3	0.7778	0.6891	0.0619	0.7271	1.1130
Synthesized d	1.8217	1.6082	1.4281	1.2736	1.1390
Optimized d	1.1000	1.0500	1.0500	1.0000	1.0000
Synthesized T_3	-0.9548	-0.7702	-0.5825	-0.3949	-0.2102
Optimized T_3	-1.0000	-0.7439	-0.5100	-0.3865	-0.2245

The performance (stability margin and resolution) of the original DT modulator and that of the synthesized modulator are compared with that of the optimized modulator including analog imperfections versus the modulator central frequency in figure 5.19. Almost 2-bits of resolution loss is a small price to pay to significantly improve the

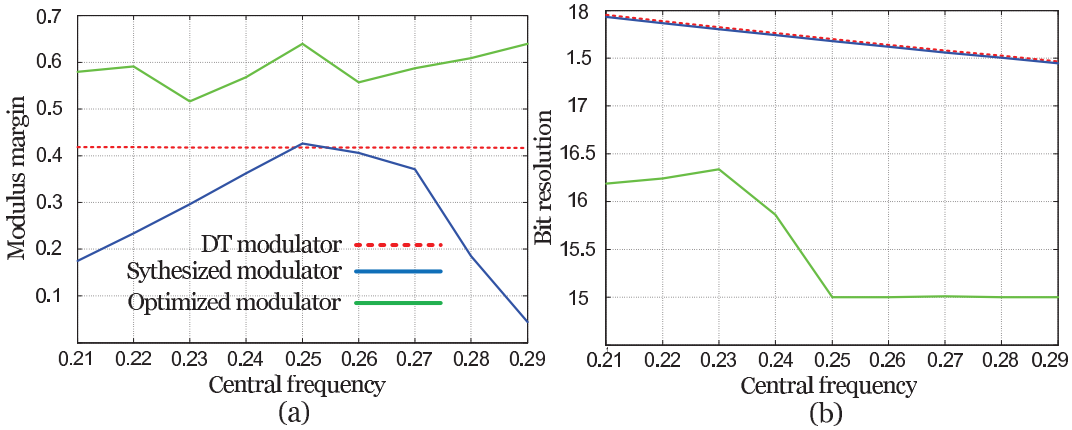

Figure 5.19: Comparison of the modulus margin (a) and the bit resolution of the optimized, synthesized and original DT modulator.

stability margin.

Since the performance of the modulator is satisfying for the worst case, the performance of the modulator is also guaranteed for imperfections less than the worst case. For $f_c = 0.29f_s$, the sensitivity of the modulus margin of the optimized modulator to C_c mismatch is shown in figure 5.20. By comparing figure 5.11 with figure 5.20, the

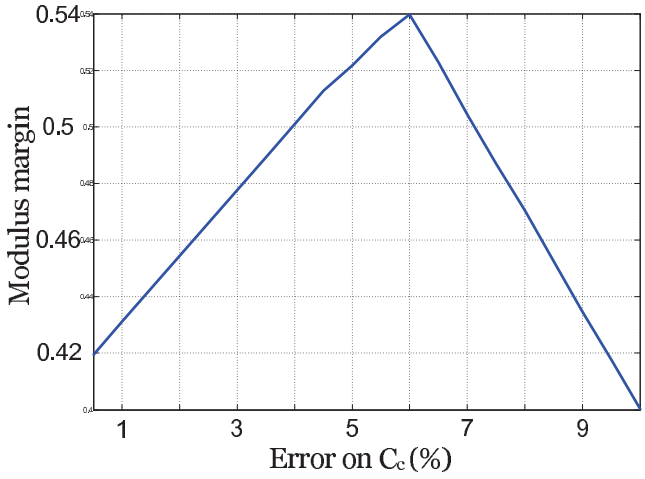

Figure 5.20: Sensitivity of the modulus margin of the optimized modulator to C_c mismatch for $f_c = 0.29f_s$.

efficiency of the proposed method is approved.

From figure 5.21 to figure 5.29 the optimized global filter and the position of the NTF poles are compared with those of the synthesized modulator for different modulator central frequencies. Moreover, the SNR and the output signal spectrum density (through the SIMULINK simulation) are shown for the optimized modulator. The spectrum of the output signal is obtained for an amplitude of the input signal equal to 0.72.

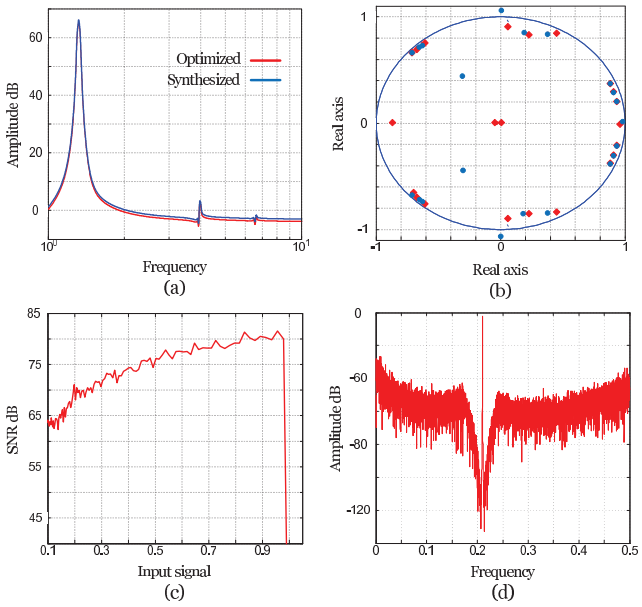

Figure 5.21: $G(s)$ (a) and the position of the NTF poles (b) for optimized and non optimized modulator. The SNR (c) and the output signal spectrum (d) for $f_c = 0.21 f_s$.

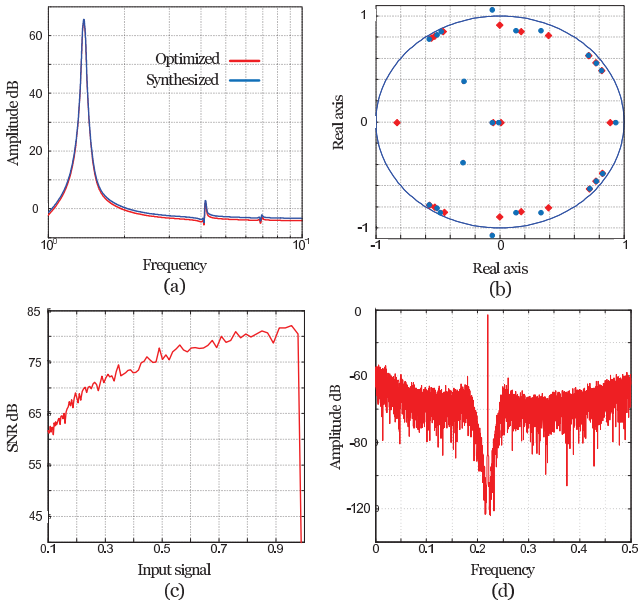

Figure 5.22: $G(s)$ (a) and the position of the NTF poles (b) for optimized and non optimized modulator. The SNR (c) and the output signal spectrum (d) for $f_c = 0.22 f_s$.

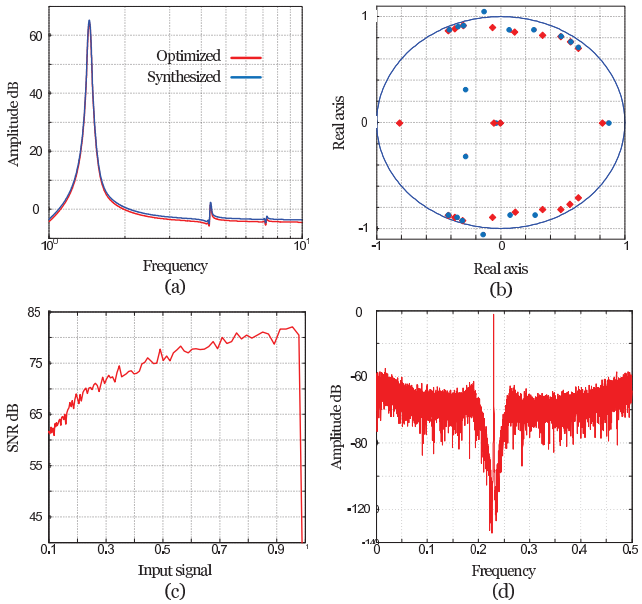

Figure 5.23: $G(s)$ (a) and the position of the NTF poles(b) for optimized and non optimized modulator. The SNR (c) and the output signal spectrum (d) for $f_c = 0.23 f_s$.

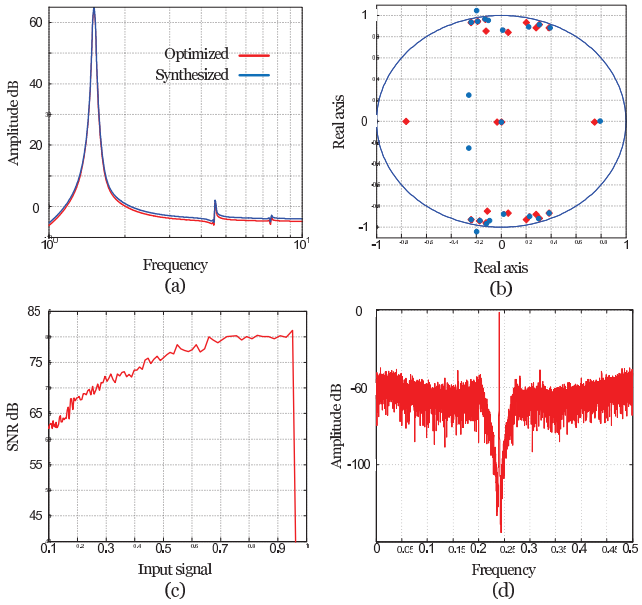

Figure 5.24: $G(s)$ (a) and the position of the NTF poles (b) for optimized and non optimized modulator. The SNR (c) and the output signal spectrum (d) for $f_c = 0.24 f_s$.

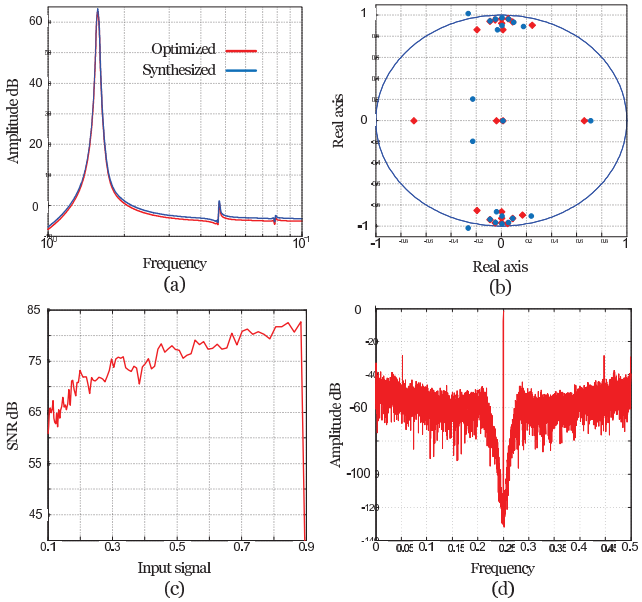

Figure 5.25: $G(s)$ (a) and the position of the NTF poles(b) for optimized and non optimized modulator. The SNR (c) and the output signal spectrum (d) for $f_c = 0.25 f_s$.

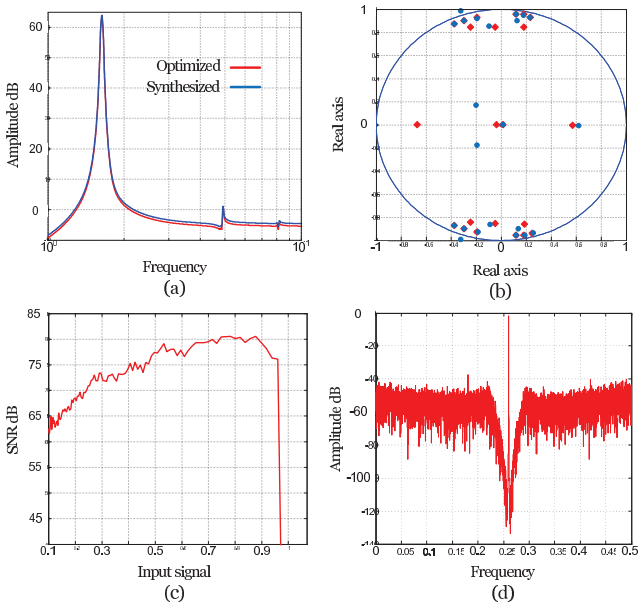

Figure 5.26: $G(s)$ (a) and the position of the NTF poles (b) for optimized and non optimized modulator. The SNR (c) and the output signal spectrum (d) for $f_c = 0.26 f_s$.

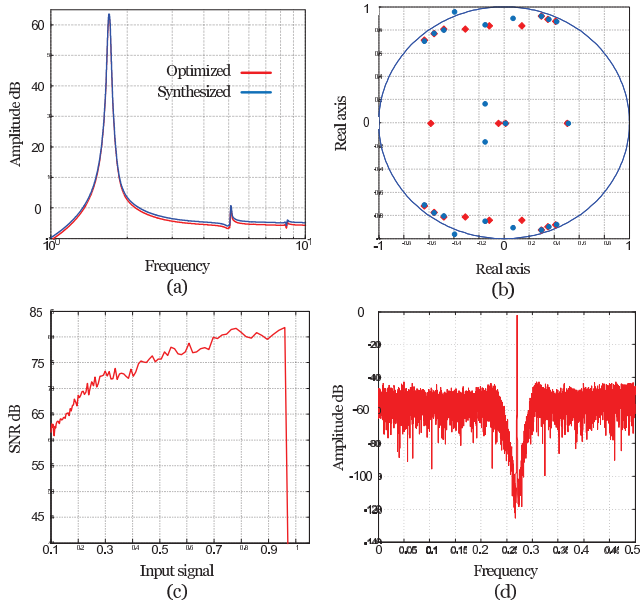

Figure 5.27: $G(s)$ (a) and the position of the NTF poles (b) for optimized and non optimized modulator. The SNR (c) and the output signal spectrum (d) for $f_c = 0.27 f_s$.

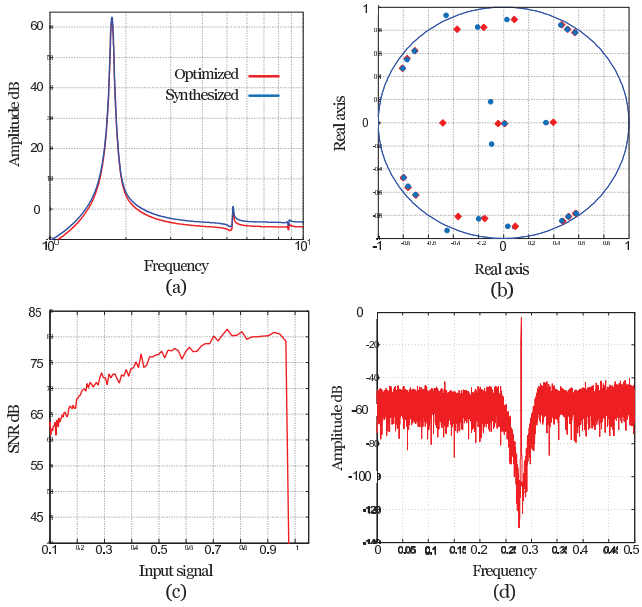

Figure 5.28: $G(s)$ (a) and the position of the NTF poles (b) for optimized and non optimized modulator. The SNR (c) and the output signal spectrum (d) for $f_c = 0.28 f_s$.

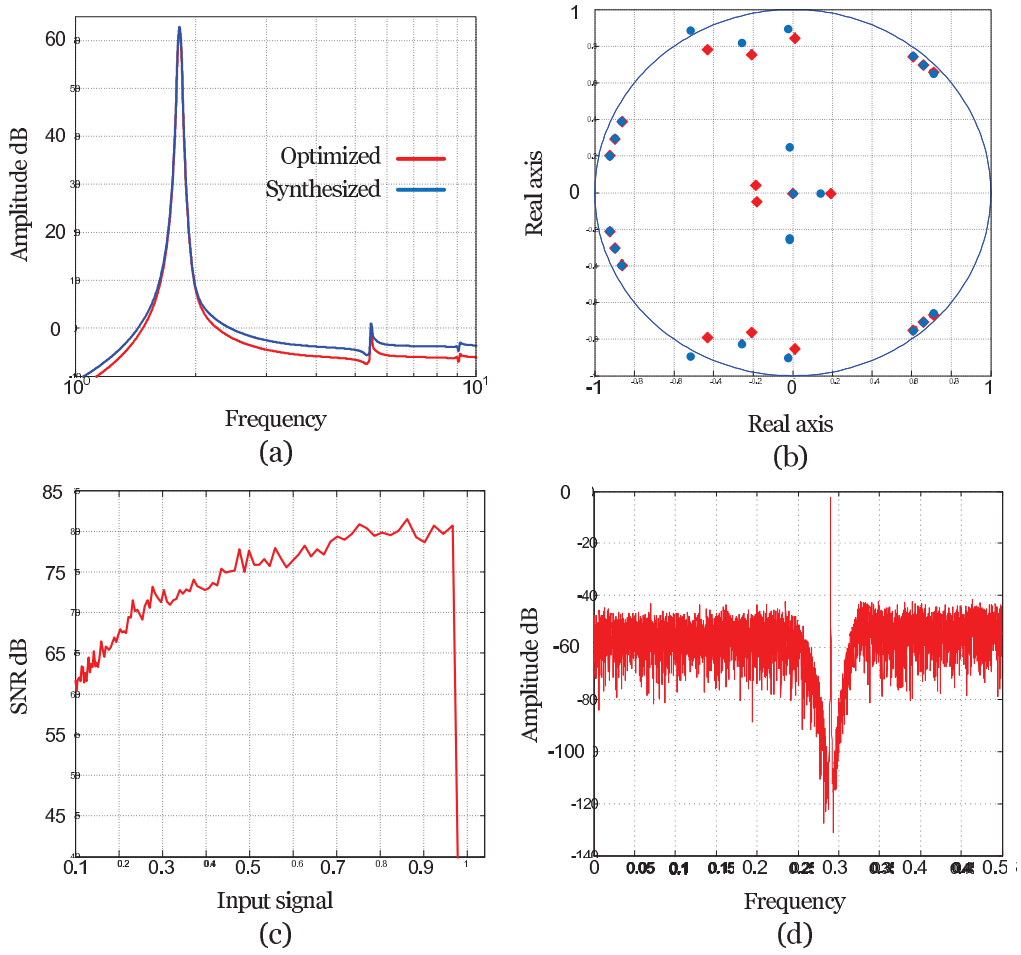

Figure 5.29: $G(s)$ (a) and the position of the NTF poles (b) for optimized and non optimized modulator. The SNR (c) and the output signal spectrum (d) for $f_c = 0.29 f_s$.

5.4 STF shaping

The STF of the topology of figure 5.8 is shown for several modulator central frequencies in 5.30. Clearly, not only the STF does not have a filtering behavior close to the modulator central frequency, but unwanted peaks may also exist at other frequencies. This is one of the major disadvantages of weighted feedforward summation structures which result in decreasing the dynamic range of the modulator.

The noise-shaping and the signal-shaping paths of the topology of figure 5.8 are coupled. This is therefore impossible to modify the STF without changing the NTF. The topology of figure 5.31 is presented to make difference between $G_x(s)$ and $G_l(s)$ (equa-

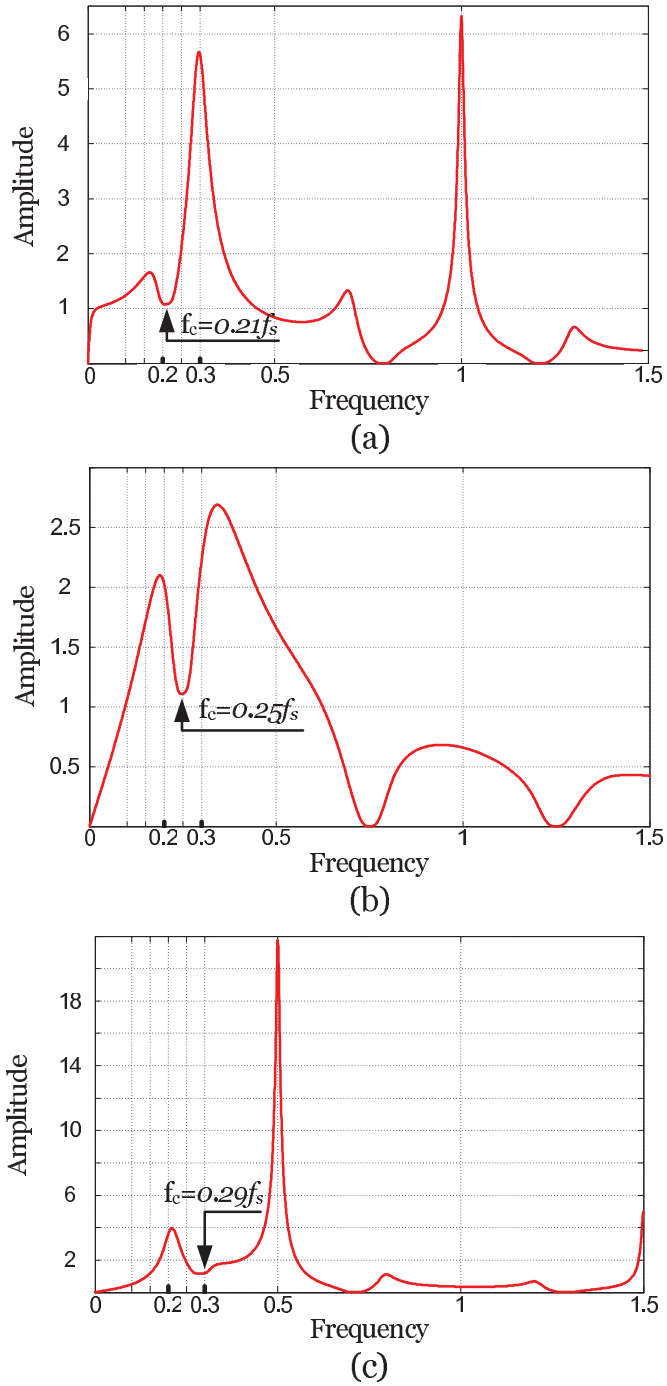

Figure 5.30: STF for $f_c = 0.21f_s$ (a), $f_c = 0.25f_s$ (b), $f_c = 0.29f_s$ (c).

tion 3.24). Therefore, by modifying k_1 and k_2 the STF is modified without modifying the NTF.

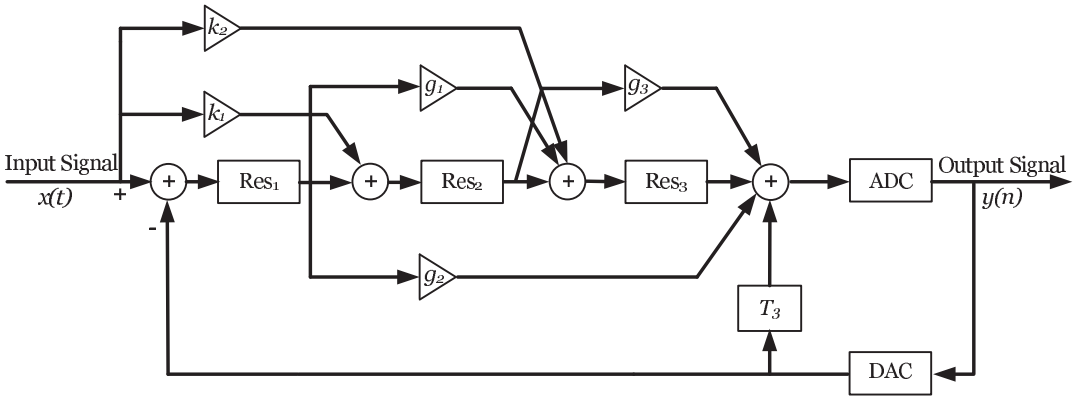

Figure 5.31: Modifiable STF topology.

Figure 5.32 is another representation of the proposed topology where g_{x1} and g_{x2} are the added signal paths. g_{x0}, g_{x1} and g_{x2} are given by:

$$\begin{cases} g_{x0} = H_{\text{Res}_1}[g_2 + g_1 H_{\text{Res}_3} + H_{\text{Res}_2}[g_3 + H_{\text{Res}_3}]], \\ g_{x1} = k_1[H_{\text{Res}_2}[g_3 + H_{\text{Res}_3}]], \\ g_{x2} = k_2 H_{\text{Res}_3}. \end{cases} \tag{5.17}$$

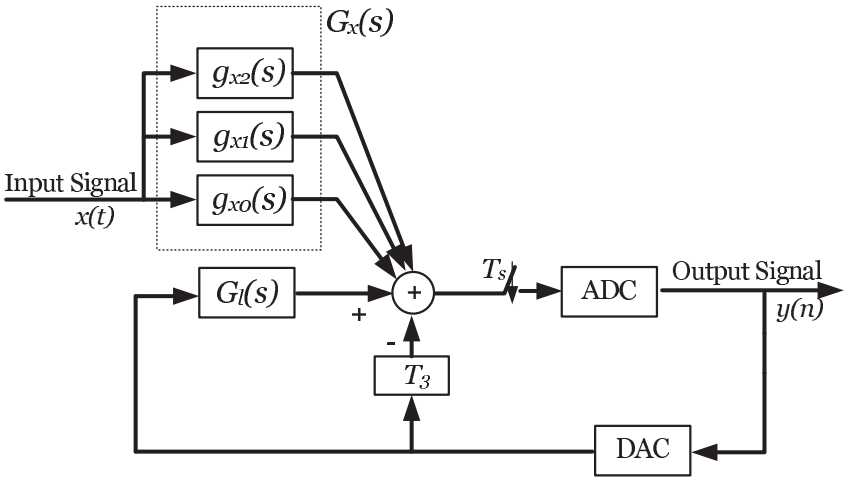

Figure 5.32: Another representation of the modifiable STF topology.

Thus, $G_x(s)$ is equal to:

$$G_x(s) = \sum_{i=0}^{2} g_{xi} \tag{5.18}$$

The STF can be calculated through equation 3.24. Although the STF should behave as a selective band-pass filter (e.g a Chebyshev II filter), with only two degree of freedom (k_1 and k_2) one can only aim at approximating the ideal STF. This can be achieved by minimizing the error between the ideal form and the practical form of the STF (figure 5.33).

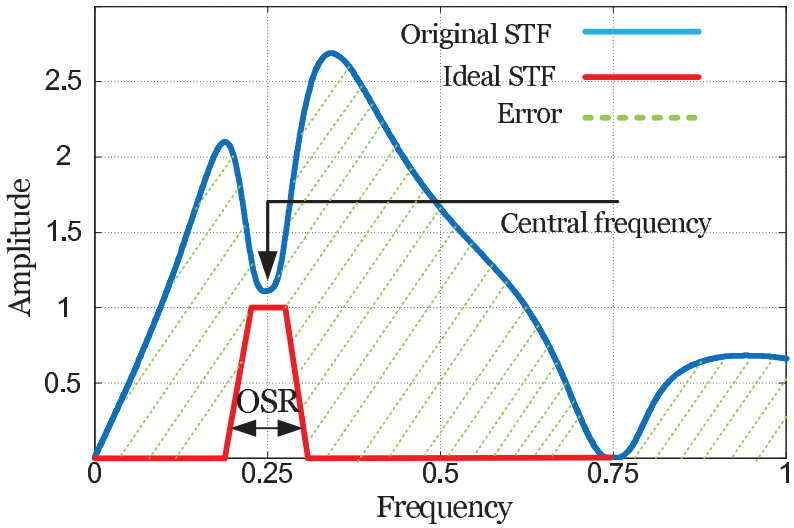

Figure 5.33: The principle of k_i optimization.

The error function is given by:

$$EF = \sum_{i=1}^{3} ef_i, \tag{5.19}$$

where ef_1, ef_2 and ef_3 are given by:

$$\begin{cases} ef_1 = \int_{f_c-\frac{\Delta f}{2}}^{f_c+\frac{\Delta f}{2}} \left(\left\| 1 - \frac{G_x(j\omega)}{1-F_l(e^{j\omega})} \right\| \, df \right), \\ ef_2 = \int_{f_c+\frac{\Delta f}{2}}^{f_s} \left(\left\| \frac{G_x(j\omega)}{1-F_l(e^{j\omega})} \right\| \, df \right), \\ ef_3 = \int_{0}^{f_c-\frac{\Delta f}{2}} \left(\left\| \frac{G_x(j\omega)}{1-F_l(e^{j\omega})} \right\| \, df \right). \end{cases} \tag{5.20}$$

The optimal values of k_1 and k_2 are shown in figure 5.34 versus the modulator central frequency.

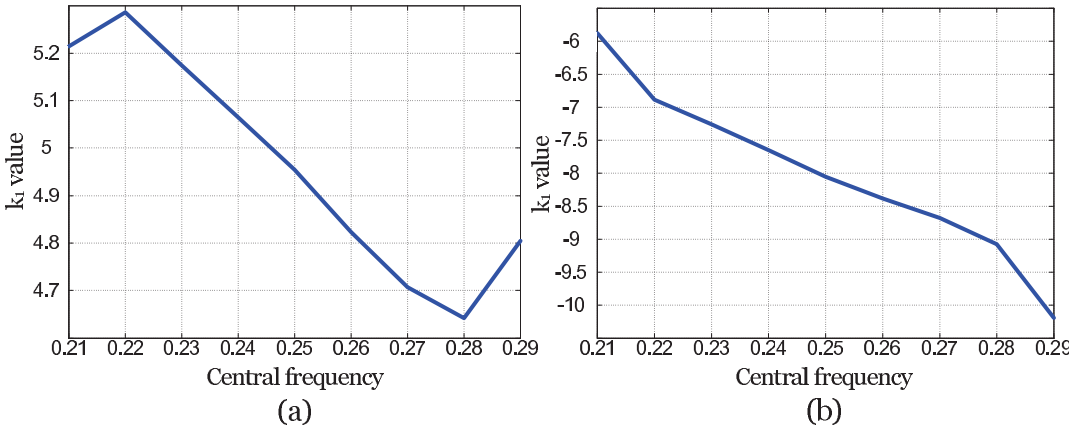

Figure 5.34: Optimal values of k_1 and k_2.

Comparing the STF of the topology of figure 5.8 and the STF of the topology of figure 5.31 proves the efficiency of this method (figure 5.36).

The sensitivity of the STF to k_1 and k_2 is shown in figure 5.35 for $f_c = 0.25 f_s$. The

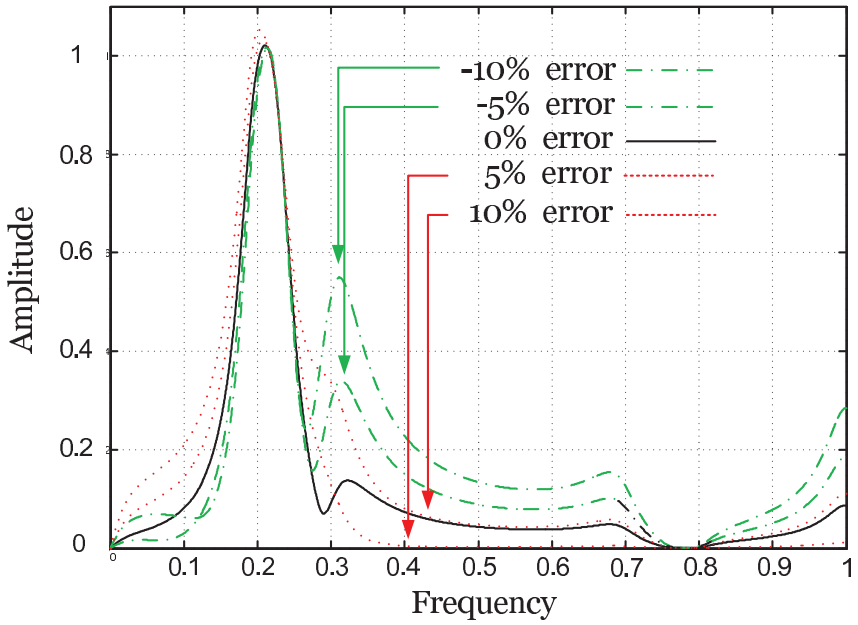

Figure 5.35: Sensitivity of the STF to variations of k_1 and k_2 for $f_c = 0.25 f_s$.

error percentage is defined by $\frac{k_{i_{\text{practical}}} - k_{i_{\text{nominal}}}}{k_{i_{\text{nominal}}}}$. As it is shown, the STF is slightly deteriorated in terms of STF central frequency. Although unwanted peaks reappears close to the modulator central frequency, their magnitudes are small.

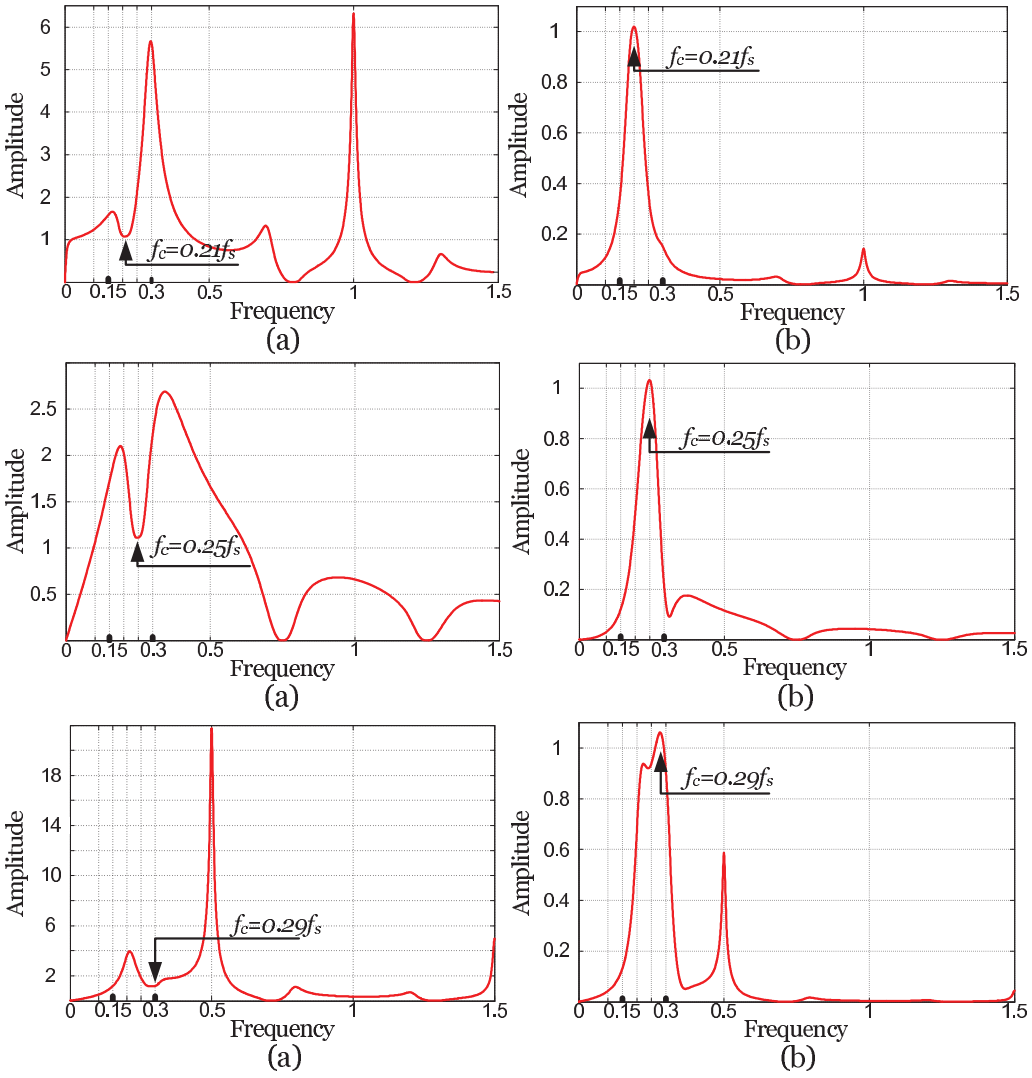

Figure 5.36: Comparing the STF before optimization when $k_1 = k_2 = 0$ (a) and after optimization (b) for several modulator central frequencies ($f_c = 0.21f_s$, $f_c = 0.25f_s$ and $f_c = 0.29f_s$).

5.5 Conclusion

EFBD systems require a modulator capable of attaining a given resolution across the frequency band of interest while high-order CT $\Sigma\Delta$ modulators are sensitive to analog imperfections regardless of the topology used to synthesize the global filter. Modifying the global filter of the modulator can be considered as a solution in order to compensate for non-idealities. For this aim, a robust topology offering an adequate control of the position of the NTF poles is required.

A new topology based on weighted feedforward techniques was proposed in this section. Although the proposed topology provides a sufficient number of degree of freedoms in order to synthesize the global filter, the DAC delay must be tuned to obtain a proper global filter. The STF of the proposed structure was also studied. It has been shown that, not only the STF does not have a filtering behavior close to the modulator central frequency but also unwanted peaks exist at neighborhood frequencies. This is one of the major disadvantages of the weighted feedforward techniques. Extra signal paths were added to the structure in order to be able to modify the STF without changing the NTF. A filtering-STF has been obtained by optimizing the coefficients of the extra signal paths.

By integrating the simple model of analog imperfections in MATLAB environment, the sensitivity of the proposed topology to analog imperfection has been studied. The results have shown that a simple synthesis of the global filter transfer function, which has been found through its DT counterpart, is not reliable in practice.

An optimization method on the modifiable parameters of the proposed topology was developed in order to recover the performance of the modulator accounting analog imperfections. The system-level models of the analog components, extracted from a transistor-level simulation, are required to ensure the performance of the fabricated modulator. Then, the optimization tool gets, as input, the the system-level model of the analog components and gives, as output, the optimized value of the modifiable parameters. The optimization method have been tested by the simple model of analog imperfections and the results were satisfying.

6

Electronic design

The schematic of the proposed 6^{th}-order single-stage feed-forward filtering-STF band-pass continuous-time $\Sigma\Delta$ modulator is presented in figure 6.1. The structure works in differential-mode to avoid common-mode problems and non-linearity issues. In the present work, p and m indicate the positive and the negative signal paths of differential-mode components .

Because of feedforward and feedback paths, there exist several nodes where the output of different components must be added together. The add function can be done easily by mixing signal paths with no need of extra enhancement in current-mode.

The modulator input is a common-mode voltage while the proposed circuit is a differential-current-mode system. Therefore, a common-mode Voltage to differential-mode Current converter (VTOC) is required. VTOC_1 provides the main input path and VTOC_2 and VTOC_3 are used to implement k_1 and k_2.

Since LWRs are passive devices, the resonator gain must be provided by an electronic control circuit. Also, low impedance connections are required to ensure the resonator Q-factor and resonance frequency. A Current to Voltage converter (CTOV) is used to convert the input current to drive voltage (as LWRs must be driven in voltage-mode) and to provide the resonator gain. The proposed schematic must be able to provide a low output impedance. The gain of CTOV_1, CTOV_2 and CTOV_3 correspond, respectively, to b_1, b_2 and b_3. The resonators output current runs into a Current to Current converter (CTOC) providing a low input impedance. Moreover, the feedforward coefficients (g_1, g_2 and g_3) are issued from CTOCs.

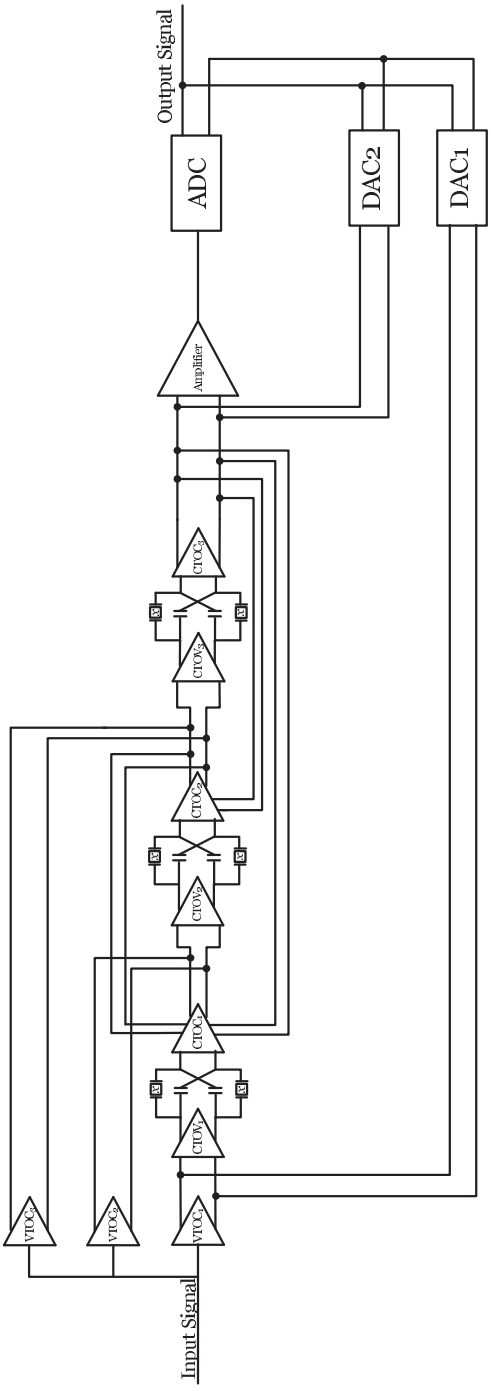

Figure 6.1: Schematic of the proposed 6^{th}-order $\Sigma\Delta$ modulator.

The sampling and the quantization function are integrated in ADC. This component is driven with a common-mode voltage. Amplifier, being a differential-mode current to common-mode voltage converter, is used for this aim. On the other side, differential-mode must be recovered in the return loop. This is less difficult to recover the differential-mode in DT domain than to do it in CT domain.
There exist various techniques to design a DAC including voltage-mode, current-mode and charge-transfer-mode techniques. Current-mode solution is chosen because the DAC output runs into nodes. Two DACs are employed to implement the main feedback and T_3.

Although the design of the required components is done in the context of a 6^{th}-order modulator, the implementation of the schematic of figure 6.1 in transistor-level is not envisaged for several reasons. The practical behavior of an LWR is unknown for us. Moreover, in our knowledge, no experimental application of LWRs in $\Sigma\Delta$ modulators is reported. Since a 6^{th}-order modulator is highly sensitive to imperfections, its design may faces several problems by employing an unknown component (LWR). On the other side, the performance of the proposed schematics in a $\Sigma\Delta$ modulator loop, must be verified in transistor-level, layout-level and a fabricated circuit. Once the reliability of the proposed solutions is approved, the design of a 6^{th}-order modulator can be envisaged.

A second-order $\Sigma\Delta$ modulator working at $f_c = 0.25 f_s$ is chosen to benchmark the solutions. A second-order modulator is more immune to analog imperfections compared with a 6^{th}-order modulator. Moreover, $T_1(z)$ is zero when working at $f_c = 0.25 f_s$ and the topology of figure 2.17 is exact.

6.1 Choice of technology

The available technology kits are:

1. AMS Bi-CMOS 0.35 μm working by 3.3 V or 5 V power supplies.
2. ST CMOS 0.13 μm working by 1.2 V, 2.5 V or 3.3 V power supplies.

Both of them are able to perform at the desired sampling frequency equal to 400 MHz. AMS has the reputation of an analog circuit technology while ST is suitable for digital applications. Although CMOS technologies are generally less consumer in terms

of chip area and cost compared with Bi-CMOS technologies, in this work the criterion of a suitable choice is the ability of designing low impedance connections to ensure the Q-factor and the resonance frequency of the resonator.

In CMOS technologies, low-impedance connections are designed by employing feedback techniques while these techniques are not useful in ST technology at desired frequency. The cut-off frequency of transistors is not sufficiently large and feedback techniques becomes instable in high frequencies. AMS technology, offering npn BJT transistors, is an alternative. The cut-off frequency of BJT transistors is in general larger than MOS transistors. Moreover, low-impedance connections can be designed by common-base (providing a low input impedance) or common-collector (providing a low output impedance) arranges. Regarding the π-hybrid model of BJT transistors (figure 6.2), the impedance seen from emitter (**E**) can be estimated by $\frac{1}{g_m} + r_e$. Although it can be reduced by increasing the transistor bias current, the power consumption of this solution is extremely large.

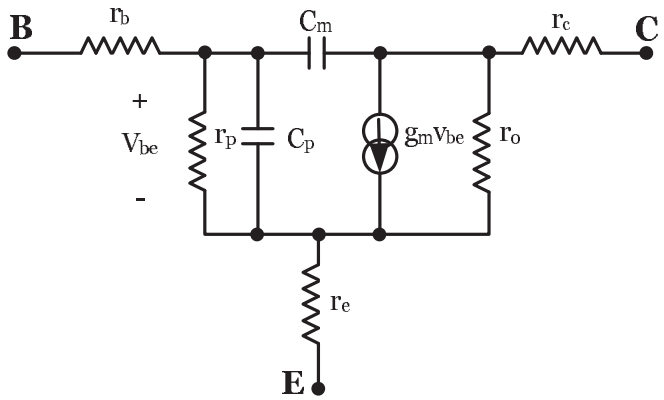

Figure 6.2: π-hybrid model of BJT transistors.

One of the major issues of integrated technologies is the large variation of device parameters in the worst case corner modeling. The worst case corner modeling is described by SPICE models and is used to ensure the circuit performance though manufacturing process. Although the parameters of a fabricated device are between the worst corners, typical mean (tm) values are used in transistor-level design. In AMS 0.35 μm kit, the following worst case corner models are defined:

- MOS transistors

1. *wp*: Fast n-MOS and fast p-MOS.
2. *ws*: Slow n-MOS and slow p-MOS.
3. *wo*: Fast n-MOS and slow p-MOS.
4. *wz*: Slow n-MOS and fast p-MOS.

- BJT transistors
  1. *hs*: High-speed high-beta BJT.
  2. *lb*: Low-speed low-beta BJT.
  3. *hb*: Low-speed high-beta BJT.
- Resistors and capacitors
  1. *wp*: Worst power.
  2. *ws*: Worst speed.
- Inductors
  1. *lq*: Low Q-factor.
  2. *hp*: High Q-factor.

Although different combinations can be produced, the two combinations given in table 6.1 are the worst cases in the context of $\Sigma\Delta$ modulators resulting the worst stability regimes. Note that no inductor is used in this circuit.

Table 6.1: The worst combinations in the context of $\Sigma\Delta$ modulators.

Combination	MOS transistors	BJT transistors	Resistors/capacitors
case 1	*wp*	*hs*	*wp*
case 2	*ws*	*lb*	*ws*

In order to illustrate the influence of the worst cases on the DC point, the gain and the cut-off frequency, a simple trans-inductance amplifier (figure 6.3) is used. T_4 and T_5 make a p-MOS bridge resistor providing the reference current. T_2 and T_3 make a n-mode current mirror and the input current (I_{in}) is converted to voltage through R_1.

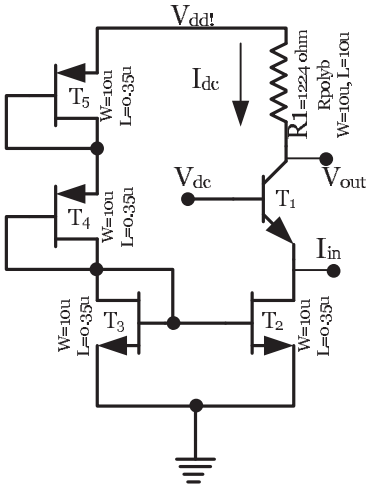

Figure 6.3: Benchmark schematic to test the influence of the worst cases.

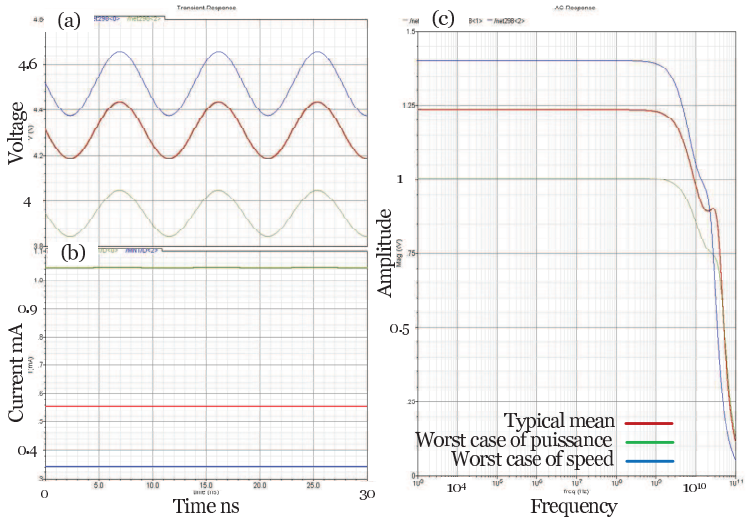

Figure 6.4: Variations of V_{out} (a), I_{dc} (b) and AC response (c) for tm and the worst cases.

The variation of V_{out}, I_{dc} and AC response of the benchmark circuit for tm values and the worst cases of table 6.1 are shown in figure 6.4. The cut-off frequency is not changed while the DC point and the gain are largely affected by almost 40% of error on R_1.

In the context of a benchmark circuit, there is no intention to design auto-correction methods in order to reduce the influence of the worst cases of the design on the performance of components. External tuning are used to compensate for analog imperfections. However the stability of the circuit must be maintained in the worst cases since if the fabricated circuit is instable, external tuning becomes useless.

The variations of bias currents and voltages can be avoided by using external current and voltage references. Also, DC-offsets are not disturbing in a differential-mode circuit as long as components are not saturated. Therefore, an extra margin for the swing of components is considered. The power supply (v_{dd}!) is set to 5 V to obtain easily the extra swing. Since the circuit is sensitive to differential-mode functionality, strict considerations on the layout design must be taken into account.

6.2 Layout rules

CT $\Sigma\Delta$ modulators are mixed-signal circuits where analog and digital circuits are implemented on a monolithic chip. High frequency signals exist in the digital part because of the clock pulses. In practice, they spread allover the circuit through parasitic capacitances of devices. this phenomena may deteriorate the performance of analog components. Isolating the digital part from the analog part is a solution to reduce the performance degradation. For this aim, the layout of the digital part (the clock generator and the digital part of the ADC) is packaged and covered by a guard ring. The guard ring is a kind of Faraday cage implemented by several metal tracks covering the digital package. The metal tracks, transporting the clock pulses, are also isolated by an extra guard ring. Moreover, the power supply and the ground of the digital part are separated from those of the analog part.

On the other side, the performance of the modulator is highly sensitive to the differential functionality. As a result, the symmetry between differential pairs must be respected in layout-level. This means the same distance from heat sources, the same width (W) and length (L) of the paired analog devices (like transistors and resistors) and the same pathway of metal tracks. Moreover, to avoid the gradient distortion of the concentration of Si doping, MOS transistors and resistors must not be extremely large in term of length or width.

The variation of devices parameters from the typical mean values may deteriorate the differential functionality if it is not symmetric between differential pairs. Selecting the same length and the same width strip for differential pairs, especially for current mirror transistors, ensures the symmetry.

The trans-impedance and trans-inductance gains are provided by resistors. Various sorts of resistors are available in AMS kit where the most linear are rpolyb and rpolyh. The last one is fabricated by a low resistive material compared with rpolyb. It is used generally to implement high-precision low-resistance resistors. Although rpolyh requires a larger dimension compared with rpolyb to achieve the same resistivity, it is less sensitive to the worst cases of the design.

Finally, in order to obtain a low impedance connection by common-collector or common-base arrange, a bias current in scale of mA is required. Therefore, the width of metal tracks transporting the bias current and the area of the corresponding transistors must be compatible with maximum currents.

6.3 Component design

6.3.1 Voltage to current converter

The schematic of figure 6.5 is proposed to convert a common-voltage-mode input to a differential-current-mode output.

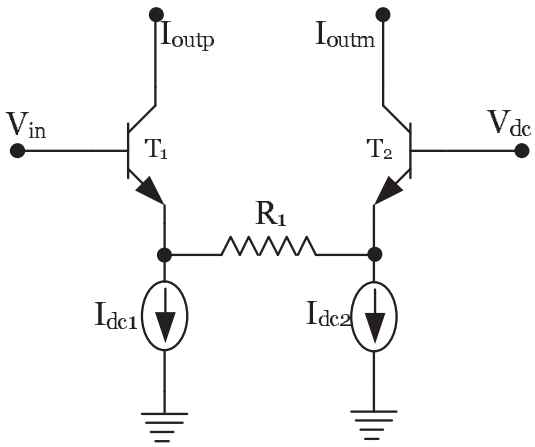

Figure 6.5: Schematic of the voltage to current converter.

The symmetry between I_{outp} and I_{outm} and their linearity is important since produced error spreads allover the modulator. As a result, BJT-transistors (T_1 and T_2) and a resistor (R_1) are employed because they have a higher cut-off frequency and a larger linearity zone compared with MOS-transistors. However, the swing of the input voltage (V_{in}) must not exceed the linearity zone of the transistors.

The symmetry between the performance of T_1 and T_2 depends on the equivalence between their bias currents. I_{dc2} is almost a steady current while I_{dc1} is an unsteady one because of the input swing. Therefore, I_{dc1} must provide a large output impedance to be immune to the input voltage swing. Finally, V_{dc} is a low noisy DC-voltage equal to the DC-offset of V_{in} to ensure the symmetry between I_{outp} and I_{outm}.

6.3.2 Current to voltage converter

The main specification concerns its output impedance. It must be sufficiently small compared with the resonator impedance at the resonance frequency. The proposed solution (figure 6.6) consists in employing a common-base arrange (T_1) to convert the input current to voltage through R_1 ($V_{out} = R_1 * I_{in}$). The value of R_1 corresponds to the required resonator gain. The output stage is a common-collector arrange (T_3) providing a small output impedance when I_{dc2} is sufficiently large.

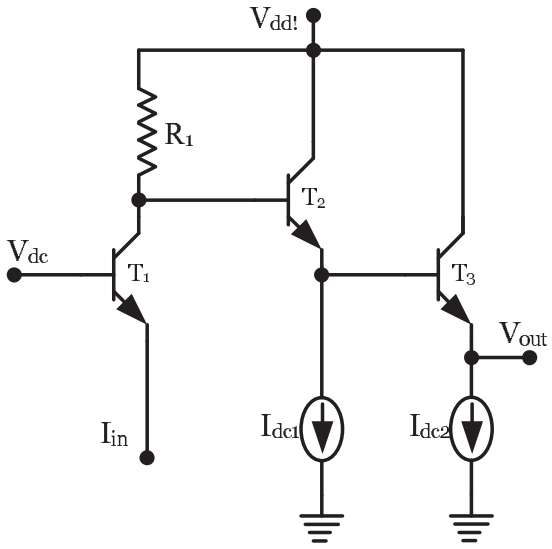

Figure 6.6: Schematic of the current to voltage converter.

The impedance of the anti-resonance cancellation path, equal to $Z_{b1} + \frac{1}{C_c s} + Z_{b2}$ (figure 4.17), is small at high frequencies. Then, when the input signal contains high frequency components the cancellation path demands a strong current and CTOV must be able to correctly provide this current for a suitable anti-resonance cancellation. This happens especially for the first resonator of the modulator (Res_1 in figure 5.8) where one of the inputs is the DAC output. The driving voltage and current of the first resonator is shown in figure 6.7. This is the results of a transistor-level simulation. The collector of T_3 is directly connected to power supply (v_{dd}!) to be able to provide the required current for charge and discharge of the anti-resonance cancellation paths. A common-collector arrange (T_2) is used to isolate T_1 from T_3. Finally, V_{dc} must be

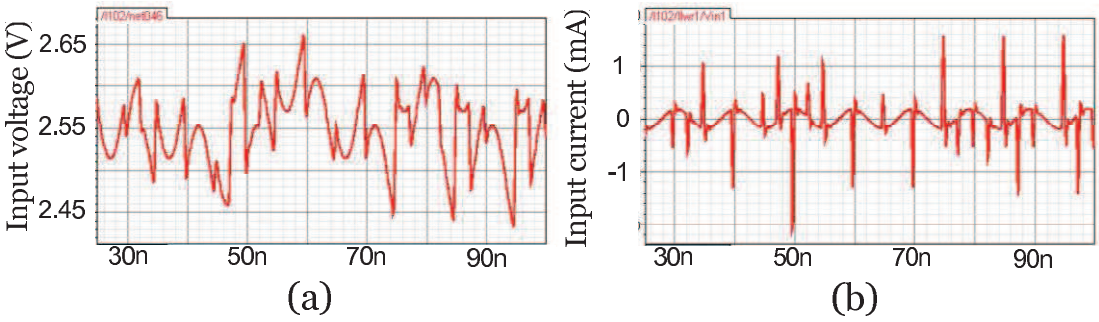

Figure 6.7: Driving voltage and current of the first LWR of the proposed structure.

optimized to ensure the swing of T_1, the connected VTOC and DAC.

6.3.3 Current to current converter

Although the same specification as the CTOV output impedance is imposed on CTOC input impedance, this is more difficult to be attained because of the peaks of the output current of LWR. Figure 6.8 presents the schematic of the proposed solution. The input stage is a common-base arrange (T_1) able to provide a low-input impedance. V_{dc}, provided by a resistor bridge, gives a noisy DC voltage because of the LWR output current peaks. Since the input impedance is equal to $\frac{\partial V_{eT_1}}{\partial I_{eT_1}}$, V_{dc} must be as steady as possible. Therefore, it is an external voltage.

The LWR output current peaks may also result in saturating the following stages and losing the main data. As a result, they must be eliminated. Since these peaks are in common-mode between I_{outp} and I_{outm} of the resonator output, they can be

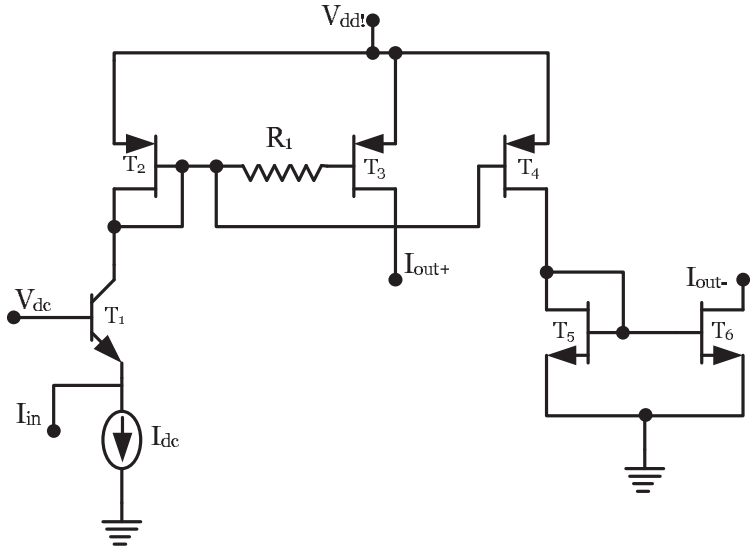

Figure 6.8: Schematic of the current to current converter cell.

removed by a differential buffer. The global view of the differential buffer is shown in figure 6.9. The proposed schematic of CTOC cells contains a n-mode current mirror

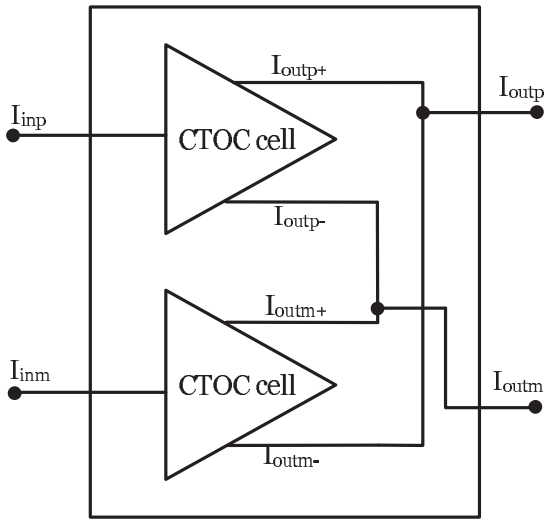

Figure 6.9: Global view of the differential buffer.

(T_5 and T_6) and a p-mode current mirror (T_2 and T_3) to obtain two inverse currents. The current path, providing I_{out-}, includes three transistors (T_4, T_5 and T_6) while that

of I_{out+} includes only one transistor (T_3). As a result, I_{out-} has a phase delay compared with I_{out+}. R_1, associated with parasitic capacitance of the gate of T_3, is used to make a low-pass filter delaying the output current of T_3.

When the optimal value of R_1 is found, I_{out+} of the negative path is in differential-mode with I_{out-} of the positive path. Adding them not only results in eliminating common-mode peaks but also the DC current issued from I_{dc} is removed.

6.3.4 Amplifier

The schematic of figure 6.10 is proposed to convert the differential-current-mode input to a common-voltage-mode output. The input stages are common-base arranges (T_1 and T_4) converting the input current to voltage through R_1 and R_5. The output stage is a differential amplifier used to eliminate common-mode distortions. Then, $V_{out} = \frac{R_2(R_1 I_{inp} - R_5 I_{inm})}{R_3}$.

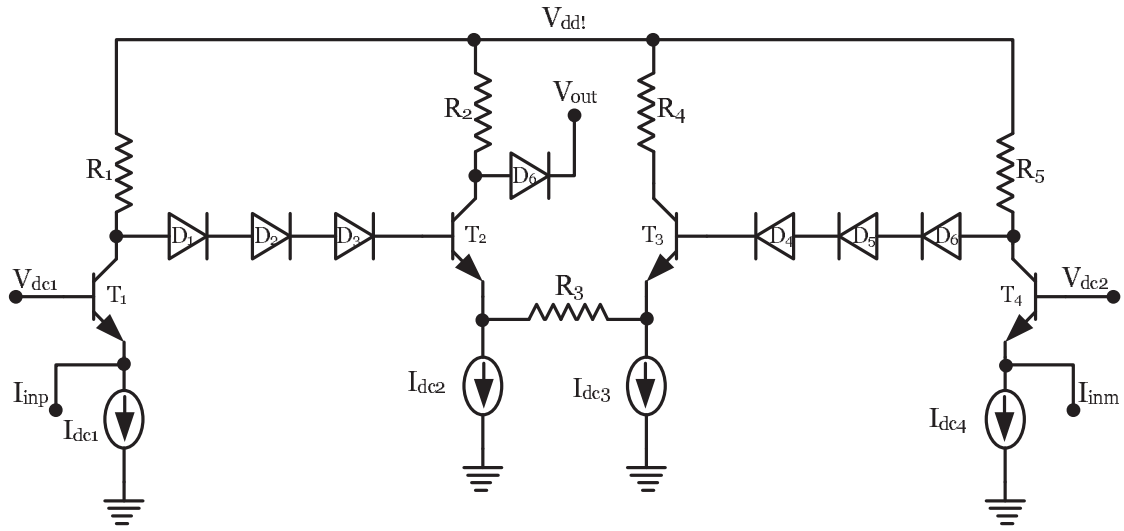

Figure 6.10: Schematic of the amplifier.

The DC point of the collectors of T_1 and T_4 is large ($v_{dd}! - R_1 * I_{dc}$) and may result in saturating the differential amplifier. Hence, the D_i stages are employed to reduce the DC level. The used schematic for the D_i stages is shown in figure 6.11.a. A diode arrange (figure 6.11.b) is not employed because the required current, for being in linearity zone, must be driven through R_1 and R_5. This complicates the DC design

of T_1 and T_4. For the same reason, the DC level of the output of the differential stage is reduced by D_6.

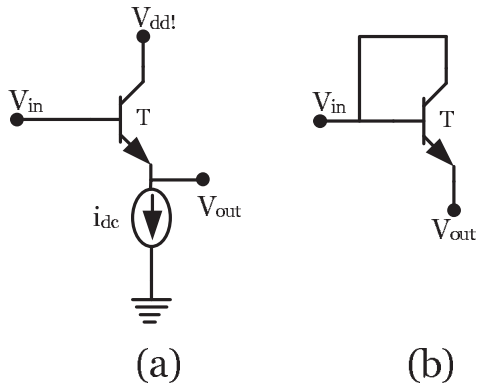

Figure 6.11: Schematic of the D_i stages (a) and a diode arrange (b).

6.3.5 Analog to digital converter

A flash ADC is chosen because of its high speed A/D conversion. The principle of a 3-bits flash ADC is shown in figure 6.12. Also, table 6.2 presents the corresponding decimal and binary representations to the ADC output.

Table 6.2: Corresponding decimal and binary representation to the ADC output.

Decimal	Binary	ADC output
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

The ADC contains $2^n - 1 = 7$ comparators, a block of threshold voltages and a rectifier system. The comparators sample and quantize the analog input signal. Their

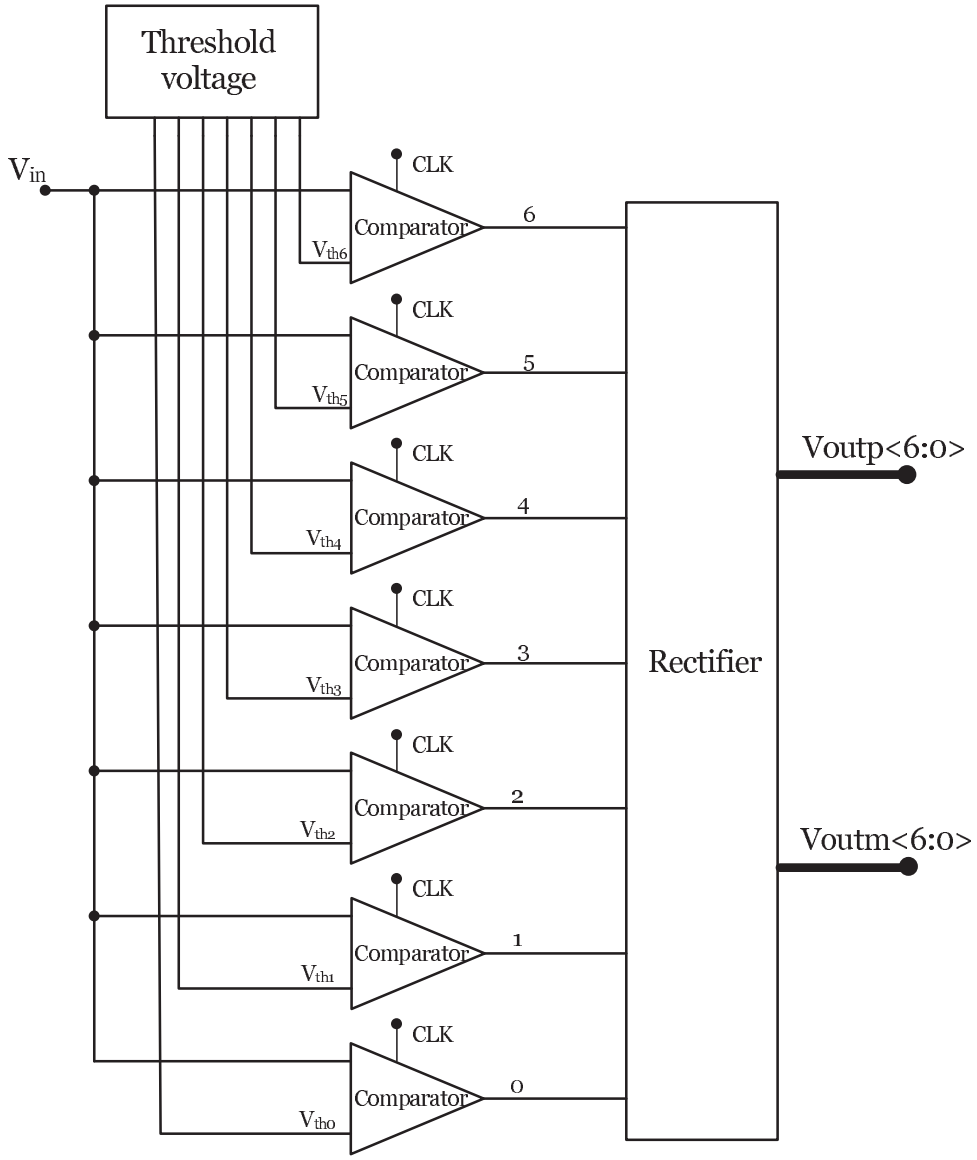

Figure 6.12: 3-bits flash ADC.

output is equivalent to a Return-to-Zero (RZ) ADC while the CT global filter is found through a Non-Return-to-Zero (NRZ) ADC function (equation 2.13). A rectifier system is used to convert the RZ output to an NRZ one. Since the performance of an NRZ ADC is sensitive to the rise-time of the clock rather than the width of the clock pulses, the design of its clock generator is less difficult than that of a RZ ADC.

The main disadvantages of the proposed ADC include large power consumption

of comparators (because of their high speed switch function) and large required chip are to implement seven comparators and the rectifier system. Moreover, the ADC is sensitive to the DC point variation of the amplifier output. The threshold voltages are set regrading the DC point of the amplifier output for the typical mean values. Then, the variation of the DC point, because of the worst cases of the design, results in a wrong decision. As a result, auto-correction methods is necessary. A constant difference between the successive threshold voltages ($V_{thi} - V_{thi-1}$ =LSB) is also required to ensure the decision results.

6.3.5.1 Comparator circuit

Voltage-mode comparators can be designed by dynamic [150], [151] or static [148], [149] techniques. Dynamic techniques are advantageous in terms of power consumption and speed compared with static techniques. The schematic of a dynamic voltage-mode comparator [152] is presented in figure 6.13.

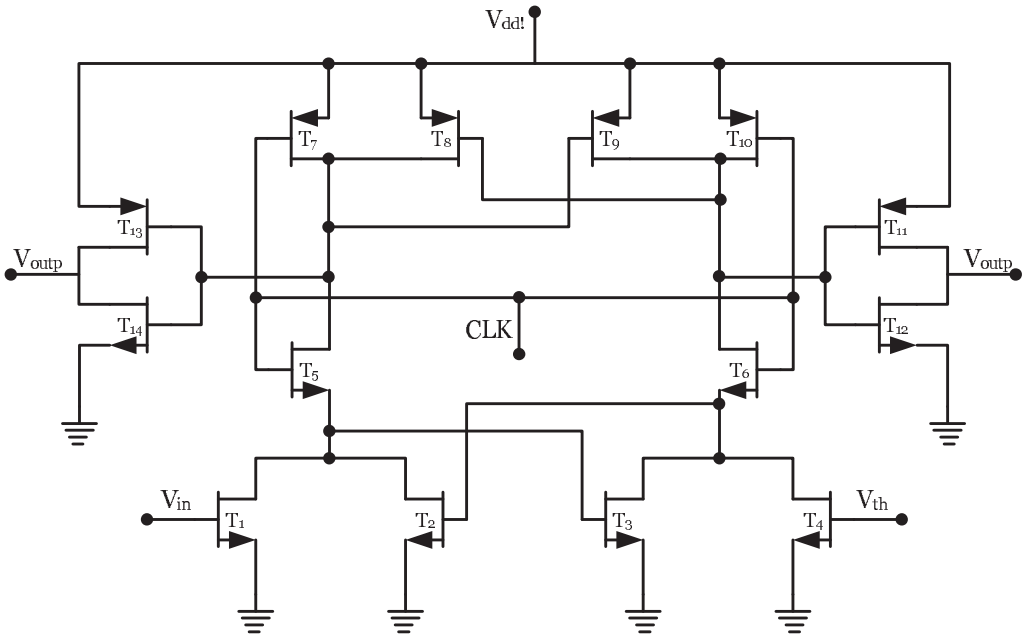

Figure 6.13: Schematic of a dynamic voltage-mode comparator.

The structure contains three stages. The input stage providing the gain, the decision stage and the output stage. The gain of the input stage ($[T_1, T_4]$) determines

the difference between V_{th} and the input signal for which the comparator switches its output level. The decision stage includes two flip-flop ($[T_2, T_3]$ and $[T_8, T_9]$) associated with charge and discharge paths ($[T_1, T_4]$ and $[T_7, T_{10}]$). Finally, the output stages are inverter gates ($[T_{11}, T_{12}]$ and $[T_{13}, T_{14}]$).
When the clock is zero ($0\ V$), T_5 and T_6 are off and the inverters input are connected to $v_{dd}!$ through T_7 and T_{10}. Consequently, the comparator output is zero. When the clock is one ($v_{dd}!$), T_5 and T_6 are saturated and their drain voltage (V_{d5} and V_{d6}) reach to a stable level because of T_2 and T_3. This level depends on the relation between V_{in} and V_{th}:

$$\begin{cases} V_{d5} = v_{dd}! \text{ and } V_{d6} = 0, & V_{in} < V_{th} \\ V_{d5} = 0 \text{ and } V_{d6} = v_{dd}!, & V_{in} > V_{th} \end{cases} \tag{6.1}$$

One may increase the size of $[T_1, T_4]$ and $[T_2, T_3]$ in order to increase the gain of the input stage. The side effect is increasing the parasitic capacitance of the input stage. This causes some problems for the amplifier since seven comparators are connected to its output. Then an optimal size of the input stage is required. Low impedance transistors are also needed to decrease the rise and the fall time of the comparators output while this results in increasing the charge and discharge peaks when the comparators change the level. Therefore, the size of the transistors must be optimized in order to find a compromise between the comparator speed and its power consumption.

6.3.5.2 Rectifier system

A differential flip-flop is used to convert the comparator RZ output to a NRZ output (figure 6.14). This structure contains two D-latch and changes the level in fall-time

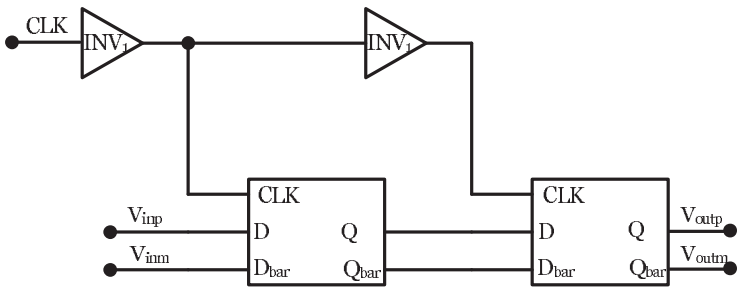

Figure 6.14: Differential flip-flop.

of the clock. Hence, it produces an internal delay equal to $1T_s$. The schematic of the employed D-latches is shown in figure 6.15.

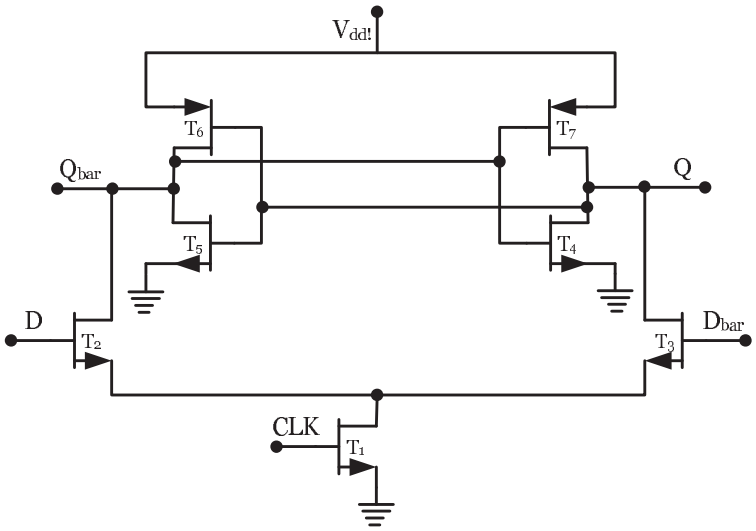

Figure 6.15: Schematic of the D-latch.

6.3.5.3 Delay

Although the rectifier introduce an internal delay equal to $1T_s$, extra delay gates are required when the loop delay is larger than $1T_s$. Since the performance of the $\Sigma\Delta$ modulator is highly sensitive to the loop delay value, modifiable delay gates are needed, in other word, the available gates in AMS technology kit are useless. The schematic of figure 6.16, containing two serried inverter ($[T_1, T_2]$ and $[T_3, T_4]$), is proposed.

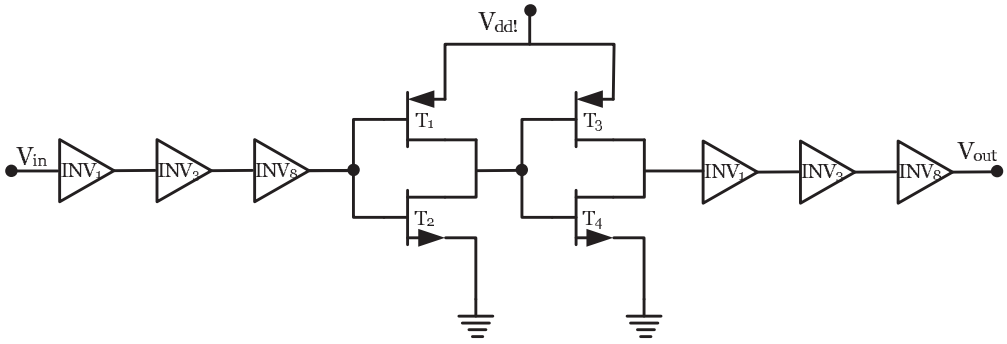

Figure 6.16: Schematic of the delay.

Inverters rise-time is larger than their fall-time because n-MOS transistors are faster than p-MOS one. Then, two inverter are serried to ensure the symmetry between the rise-time and the fall-time of the delay output. Increasing the delay is done by increasing the parasitic capacitance of the inverters. A large delay is the result of a large input parasitic capacitance while the latch output stage is not able to drive a large capacitance. Although a small inverter providing a low parasitic input capacitance is suitable also to isolate the latch stage, it is not able to directly drive a large parasitic capacitance. Therefore, a chain of inverters (INV1, INV3 and INV8) is used in the entrance. Because of the capacitive behavior, the delay output has not a sharp rise and fall time. The output stage (INV1, INV3 and INV8) is employed to rectify the output form.

6.3.5.4 Clock

The generation of the clock signal is based on the oscillation of an instable looped system (figure 6.17) where the loop contains an even number of inverters. The resulted oscillation is filtered through the parasitic capacitance of transistors ($[T_1..T5]$). Since the frequency of the produced clock signal depends to parasitic capacitance, it can be modified by modifying the transistors size ($\frac{W}{L}$) and the bias voltage (V_{dc}).

The clock generator is not able to drive directly several corresponding nodes. Connecting several nodes to the clock generator results in a large capacitive behavior reducing the rise and fall time of the clock signal. This may cause some prolems since the ADC is sensitive to the clock rise-time. A clock tree system is used ensure a small symmetric capacitive behavior at each node. However, the required chip area is extremely large.

6.3.6 Digital to analog converter

The principle of digital to analog conversion (DAC cell) is shown in figure 6.18. The level of output currents depends on the relation between V_{dc1} and the level of the input voltage. Assuming that V_{inp} is 1 ($V_{inp} = 5\ V$), T_1 is saturated and when V_{dc1} is sufficiently small, T_2 is off. As a result, I_{dc1} is passing through T_1 and $\mathrm{I_{outm}}$ is zero. On the other side, V_{inm} is 0 ($V_{inp} = 0\ V$). Then T_4 is off and when V_{dc1} is enough large to make T_3 saturated, $\mathrm{I_{outp}}$ is equal to I_{dc2}.

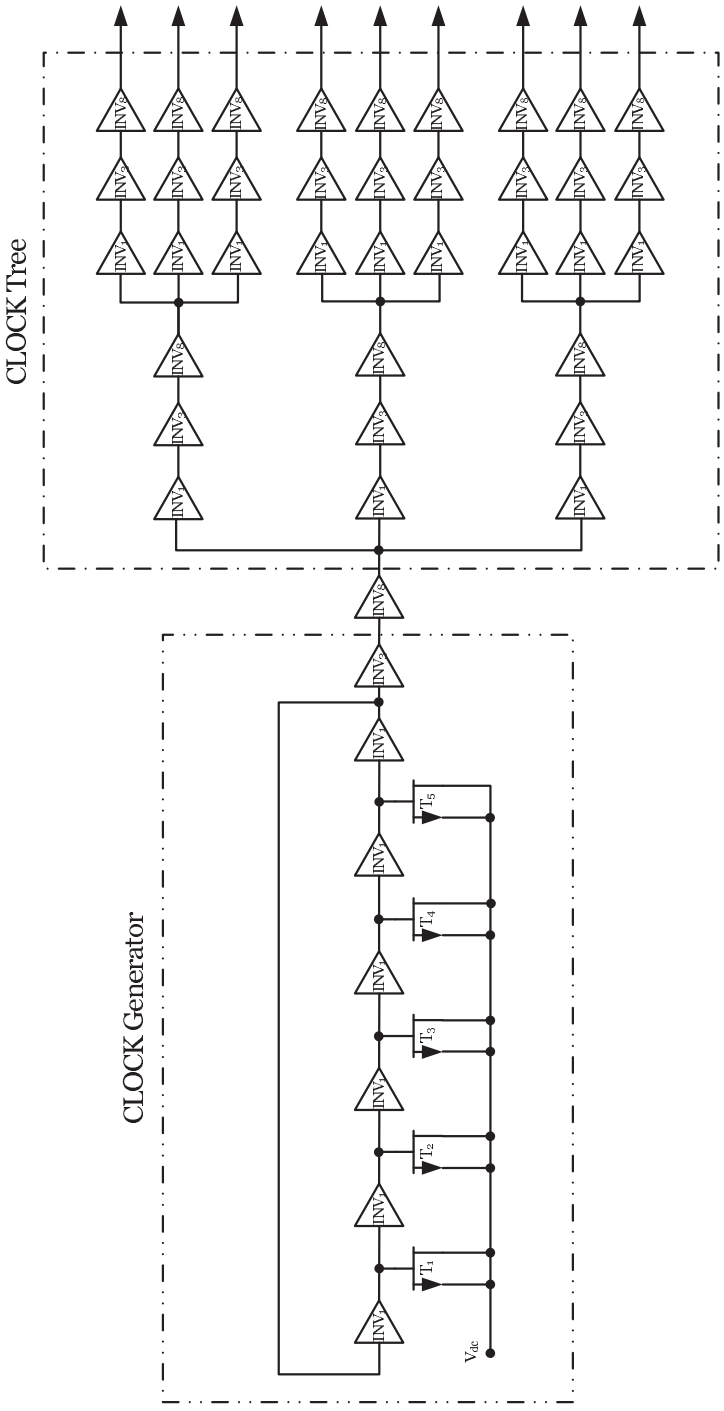

Figure 6.17: Schematic of the clock generator and the clock tree.

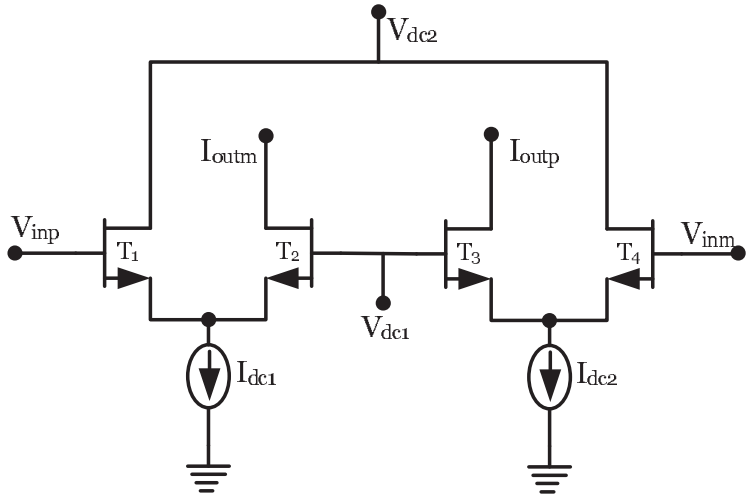

Figure 6.18: Schematic of the DAC cell.

When V_{dc1} is very large, T_2 and T_3 are keeped saturated all times. Then, I_{dc} is divided between $[T_1, T_2]$ and $[T_3, T_4]$. On the other side, when V_{dc1} is very small, output current peaks appear at switching times. V_{dc2} has the same influence and an optimal value of them is required.

Figure 6.19 presents the global topology of the DAC. Seven cells are put in parallel

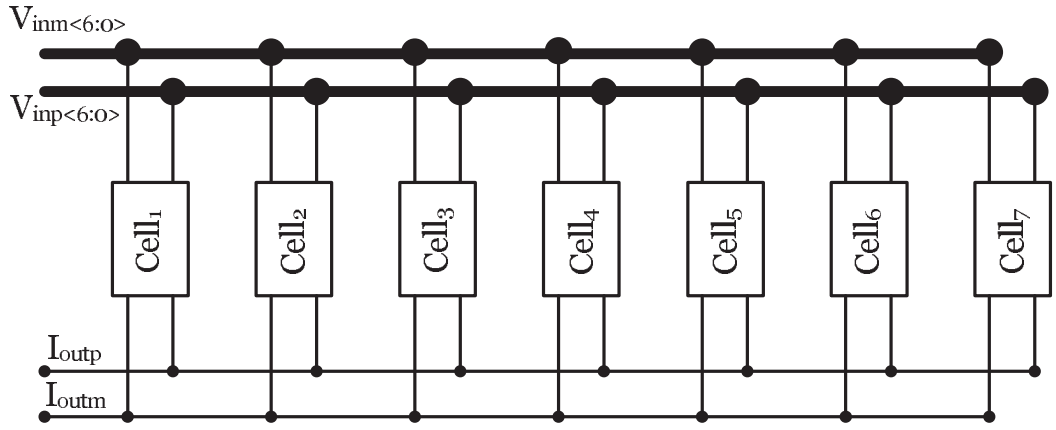

Figure 6.19: Global topology of digital to analog converter.

where each of them process one of the ADC outputs. The full-scale current (I_{fs}) is divided by seven and the I_{dc} of each cell is equal to $\frac{I_{fs}}{7}$. When $V_{inp} < 6:0 >$ is equal

to [1111111] and consequently $V_{inm} < 6:0 >$ is equal to [0000000], I_{outp} becomes equal to I_{fs} and I_{outm} is zero.

6.3.7 DC current sources

Various sorts of current mirror are presented in figure 6.20. A current mirror is characterized by its output impedance and its parasitic capacitance. The length (L) and the width of transistors are used to modify the characteristics of a current mirror. Figure 6.20.a is a simple n-mode current mirror. Although it is not able to provide a large output impedance, it is employed when a small parasitic capacitance is of primary importance. In figure 6.20.b, two pairs of transistors are put in cascade to increase the output impedance while the the parasitic capacitance is also increased.

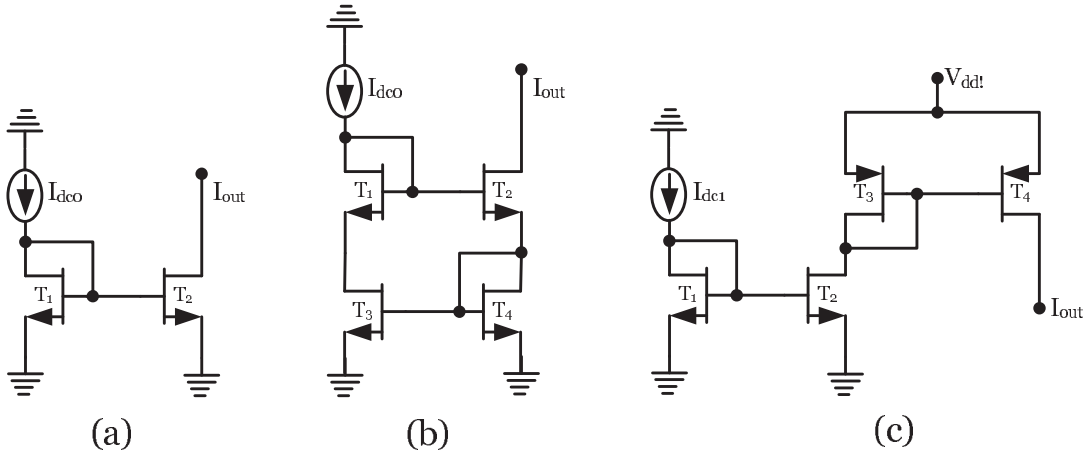

Figure 6.20: Simple n-mode current mirror (a) Cascade n-mode current mirror (b) and n-mode to p-mode current converter (c).

In order to reduce the issue of DC point variation, because of the worst cases of the design, an external n-mode current reference is used and all the bias currents are reflected from the reference. Figure 6.20.c is used when a p-mode current is required.

6.3.8 DC voltage sources

Since a resistor bridge (figure 6.21.b) requires a large chip area and a large power consumption, resistors may be replaced by p-MOS transistors (figure 6.21.a). In order to ensure the DC point constancy at worst cases of the design, the length (L), width

(W) and the width strip of transistors must be the same. p-MOS resistor bridges are useless in two cases. First, when a large current is required from the bias voltage and also when it is not possible to provide the required V_{ds} of p-MOS transistors. Then resistor bridges remains as the unique solution.

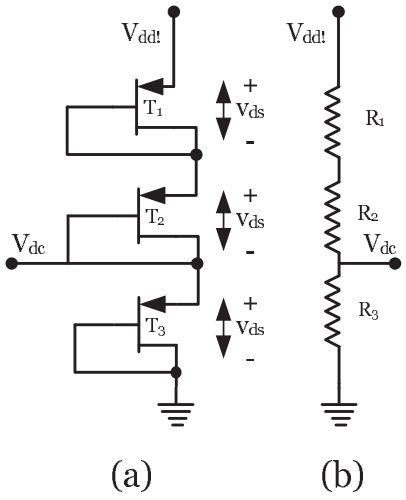

Figure 6.21: p-MOS transistor resistor bridge (a) and resistor bridge (b).

6.4 Design of a second-order single-stage sigma-delta modulator working at $f_c = 0.25 f_s$

Figure 6.22 presents the structure of a second-order single-stage ΣΔ modulator. The

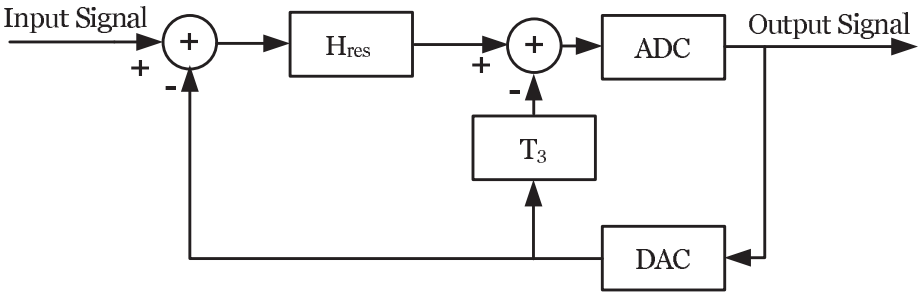

Figure 6.22: Second-order single-stage ΣΔ modulator.

DAC delay for which the global filter has no constant term in the numerator is equal

to $1.5T_s$. Then the loop filter transfer function is calculated through equation 2.13 and is given by:

$$G(s) = \frac{0.354s}{s^2 + \frac{2\pi f_c}{Q}s + (2\pi f_c)^2}, \tag{6.2}$$

where $f_c = 0.25f_s$ and $Q = 75$ and T_3 is equal to 0.25. Note that for a second-order modulator, $G(s)$ and H_{res} are the same.

The schematic of the second-order modulator is illustrated in figure 6.23. The full-scale voltage and current are given by:

$$\begin{cases} V_{fs} = \pm 0.25\ V, \\ I_{fs} = \pm 100\ \mu A. \end{cases} \tag{6.3}$$

They are neither very large to avoid the electronic device non-linearity zone and nor very small to be affected by the internal noise of electronic devices.

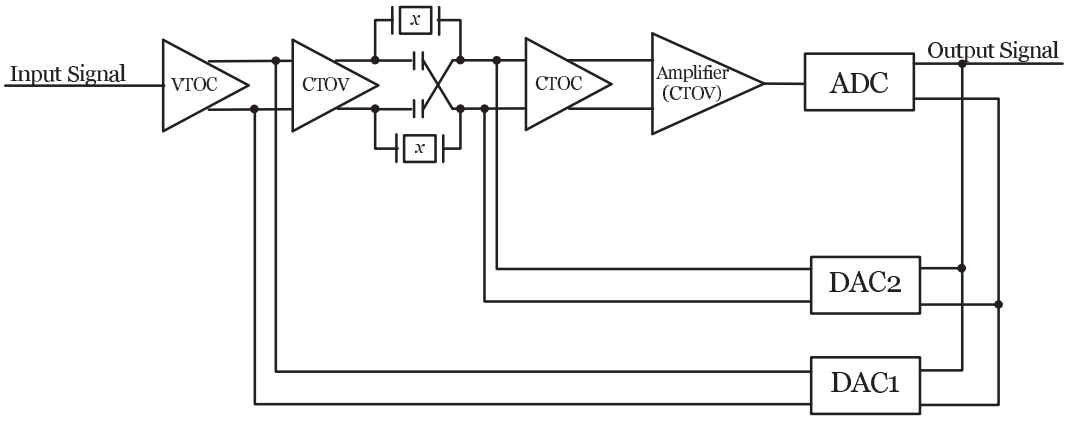

Figure 6.23: Schematic of the second-order modulator.

6.4.1 Voltage to current converter

The objective is converting a common-voltage-mode input ($\pm 0.25\ V$) to a differential-current-mode output ($\pm 100\ \mu A$). The DC-offset of V_{in} is set equal to 2.25 V to be an adequate bias voltage for I_{dc}. Figure 6.24 shows the linearity of the output currents for different values of I_{dc1} and I_{dc2}. The linearity is the derivate of the output current for a ramp input voltage varying between $V_{in_{min}} = 2\ V$ and $V_{in_{max}} = 2.5\ V$ in a DC simulation. For an ideal linear system, the derivate of the output current is a constant

value. I_{outp} is not as linear as I_{outm} because of V_{in} variation. The optimized devices characteristics are listed as follows:

- $R_1 = 2307\Omega$ (rpolyh $W = 8\mu\ m$, $L = 15\mu\ m$).
- T_1 and T_2: npn111h5, area=0.8.
- $I_{dc1} = I_{dc2} = 500\ \mu A$.

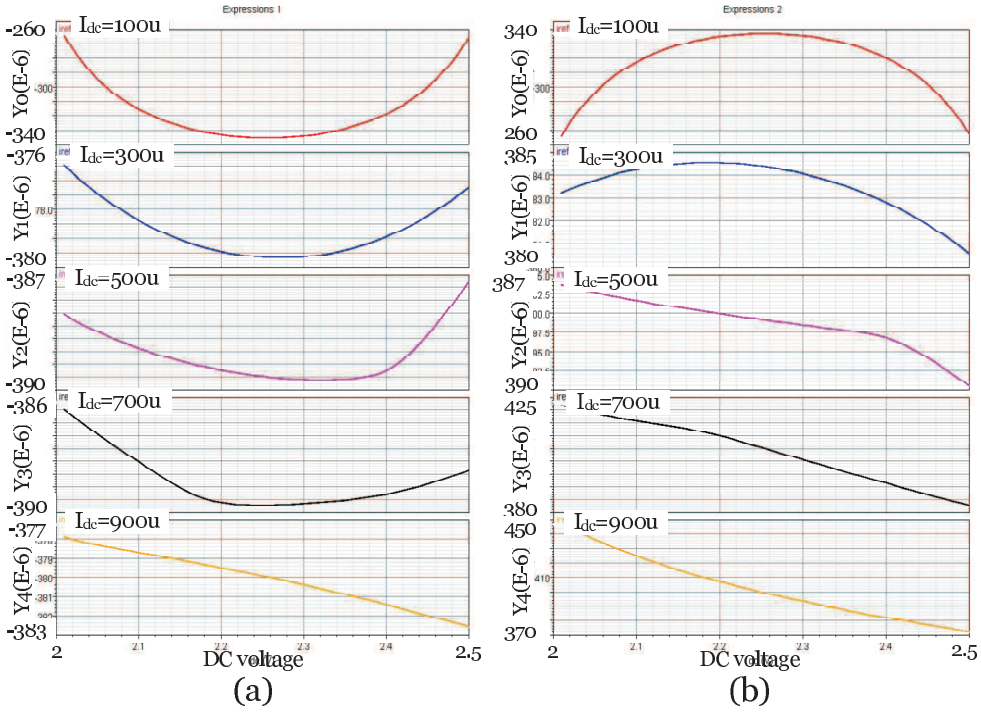

Figure 6.24: Linearity ($\frac{\partial I_{outp}}{\partial V_{in_{dc}}}$) of VTOC output ($I_{outp}$ (a) and I_{outm} (b)) for different bias currents.

Figure 6.25 presents the transient response of the DC currents (a) and the output currents (b), the AC response (c) and the DC response of the output currents. The bias currents are immune to the worst cases of the design while the trans-inductance gain is affected (figure 6.25.c). This is because of the variations of R_1 in the worst cases of the design. This may result in deterioration of the modulator performance.

Figure 6.26 shows the layout of the VTOC circuit. The large device, compared with other devices, in the center of the layout is R_1. Visibly, the required chip area of a resistor is extremly large.

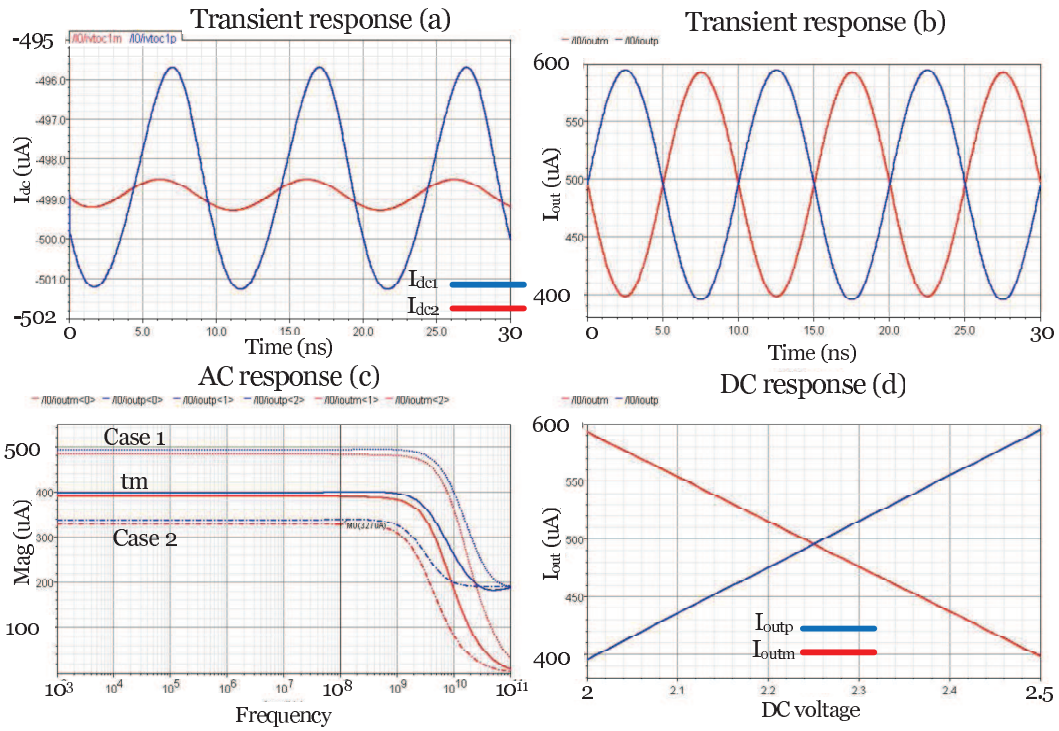

Figure 6.25: Transient response of DC currents (a) and the output currents (b), the AC response (c) and the DC response of the VTOC output currents.

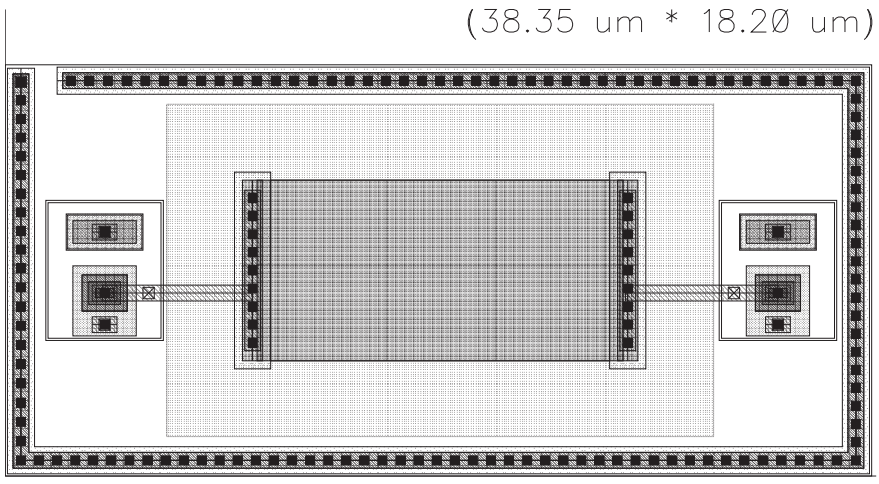

Figure 6.26: Layout of the VTOC circuit.

6.4.2 Current to voltage converter

The required resonator gain is equal to 0.35. Hence, R_1 is almost equal to $\frac{0.35}{\pm 100\ \mu A}$. V_{dc} is set to 3.8 V to provide an adequate swing for T_1 and the output stage of the VTOC. It is provided by a resistor bridge (R_2 and R_3). The optimized devices characteristics are listed as follows:

- $R_1 = 1754\Omega$ (rpolyh $W = 8\mu\ m$, $L = 11.4\mu\ m$), $R_2 = 3168\Omega$ (rpolyb $W = 1\mu\ m$, $L = 13.2\mu\ m$), $R_3 = 8976\Omega$ (rpolyb $W = 1\mu\ m$, $L = 37.4\mu\ m$).
- T_1 and T_2: npn111h5, area=0.8, T_3: npn111h5, area=$0.8 * 8$.
- $I_{dc1} = I_{dc2} = 250\ \mu A$, $I_{dc3} = 1.5\ mA$.

The unloaded circuit is tested with a pure sinusoidal input at 100 MHz. The results are shown in figure 6.27. Although in the worst cases simulations the output DC level

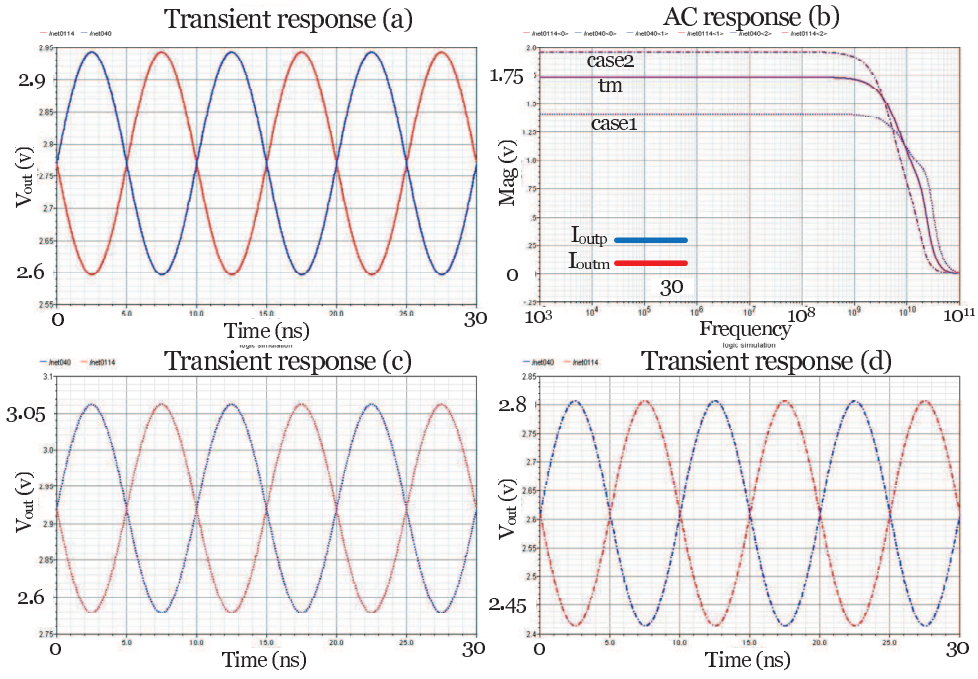

Figure 6.27: Transient response of the output voltage for the typical mean values (a), the first worst case (c) and the second worst case (d) and the AC response for the same cases for the unloaded CTOV.

is changed, it is not important as long as the transistors are not saturated because

the following stage is an band-pass resonator being an open-circuit at DC. The loaded circuit by LWR is also tested for the same input combined with a pulse signal (figure 6.28.a). The results are shown in figure 6.28. Although in the rise and fall time of the

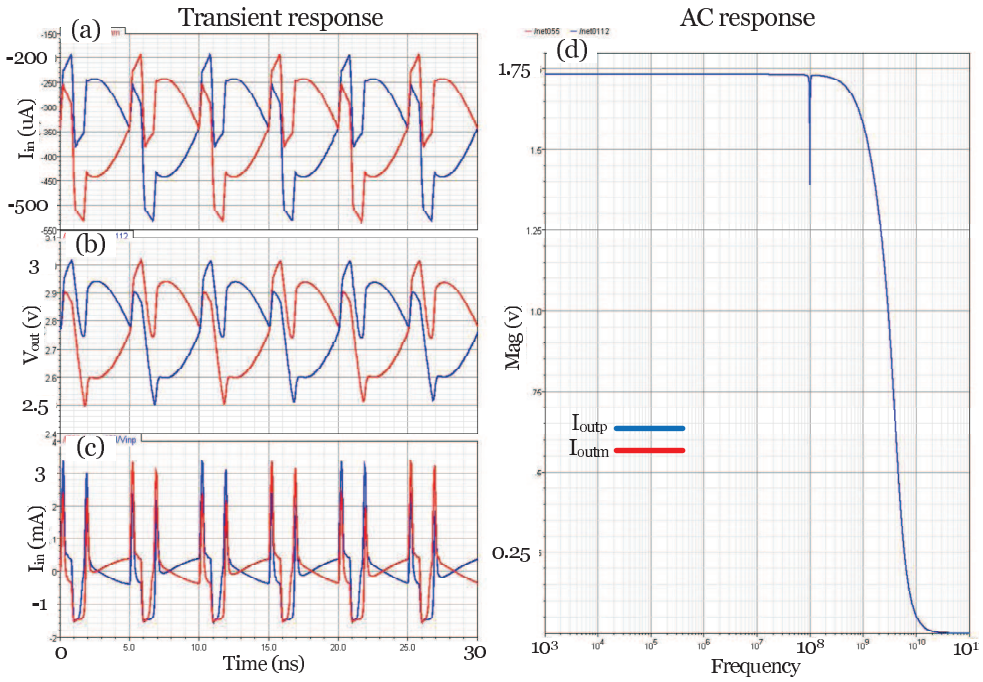

Figure 6.28: Transient response of the input current(a), the output voltage (b) and the output current (c) of the loaded CTOV and its AC response (d).

input pulse wave, the charge and discharge of the cancellation paths demand a large current (figure 6.28.c), the current peaks are in common-mode between differential paths. On the other side, the AC gain is reduced at working frequency (100 MHz). This means that the output impedance of CTOV is not sufficiently small. Regarding the value of I_{dc2} (equal to 1.5 mA), increasing I_{dc2} to reduce the output impedance is not a good solution. Increasing the trans-impedance DC gain is an alternative since the magnitude shoot is not large.

Figure 6.29 shows the layout of the CTOV circuit. Visibly, the symmetry between the differential pairs are strictly respected to maintain the symmetry between the output current peaks.

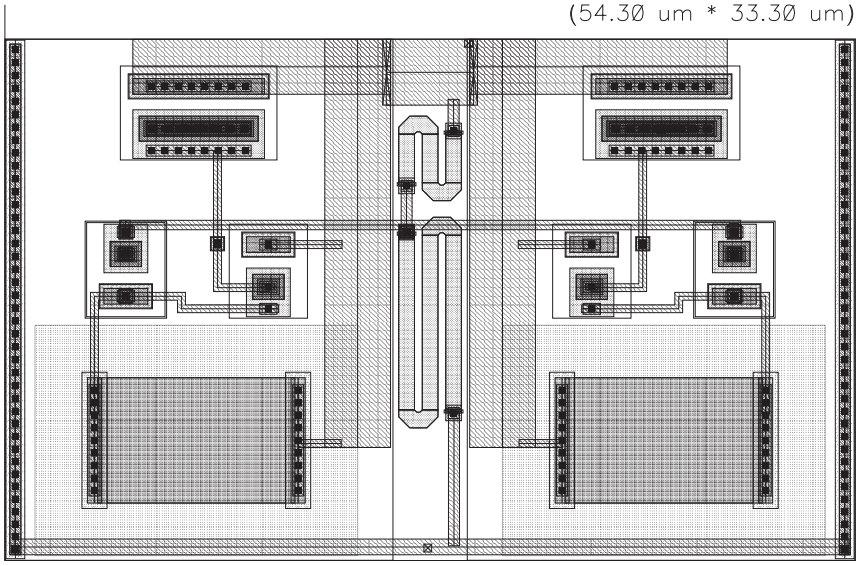

Figure 6.29: Layout of the CTOV circuit.

6.4.3 Current to current converter

Figure 6.30 shows the positive output (I_{outp}) of the CTOC for different values of R_1 when the input current is the LWR output shown in figure 6.28.c.

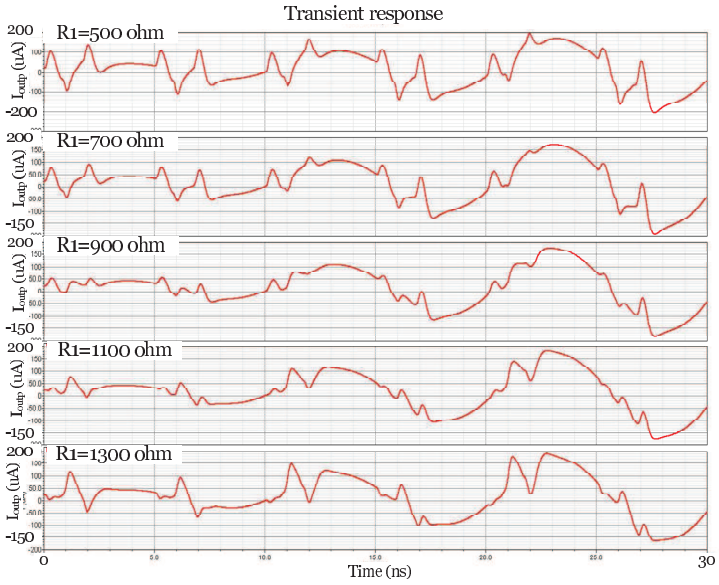

Figure 6.30: CTOC output for different values of R_1.

When R_1 is not correctly set, I_{out+} and I_{out-} are not in the same phase and the current peaks are not correctly eliminated. Remember that I_{outp} is equal to the sum of the I_{out+} of the positive path and the I_{out-} of the negative path of the differential CTOC (figure 6.9). The optimized devices characteristics are listed as follows:

- $V_{dc} = 3\ V$ and $V_{dc_{out}} = 2.25\ V$.
- $R_1 = 900\ \Omega$ (rpolyb $W = 5\ \mu m$, $L = 18.75\ \mu m$).
- T_1: npn254h5, area=$3.2 * 8$.
- T_2: $\frac{W}{L} = \frac{60\ \mu m}{1\ \mu m}$, T_3 and T_4: $\frac{W}{L} = \frac{30\ \mu m}{1\ \mu m}$, T_5 and T_6: $\frac{W}{L} = \frac{20\ \mu m}{1\ \mu m}$,
- $I_{dc} = 1.5\ mA$.

In figure 6.31, the CTOC output for a pure sinusoidal input at 100 MHz is compared with the CTOC output for the same input combined with a pulse signal. The input

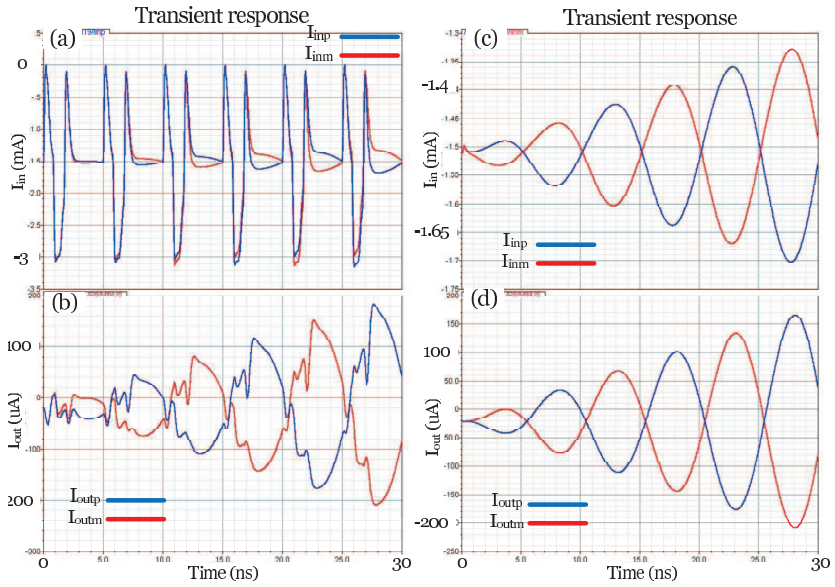

Figure 6.31: Input current(a) and the output current (b) of CTOC for an input signal containing a pure sinusoidal current at 100 MHz combined with a pulse signal and the input current(c) and the output current (d) of CTOV for a pure sinusoidal input at 100 MHz.

signal is applied to CTOV loaded by LWR loaded by CTOC. The AC response of the CTOC is shown in figure 6.32.a. The frequency band of CTOC is not large because of

employing p-MOS transistors. The influence of the worst cases of the design is shown in figure 6.32.b. Because of the variations of R_1, the current peaks are not correctly removed in the worst cases of the design. Figure 6.29 is the layout of the CTOC circuit. The symmetry between differential pairs is strictly respected.

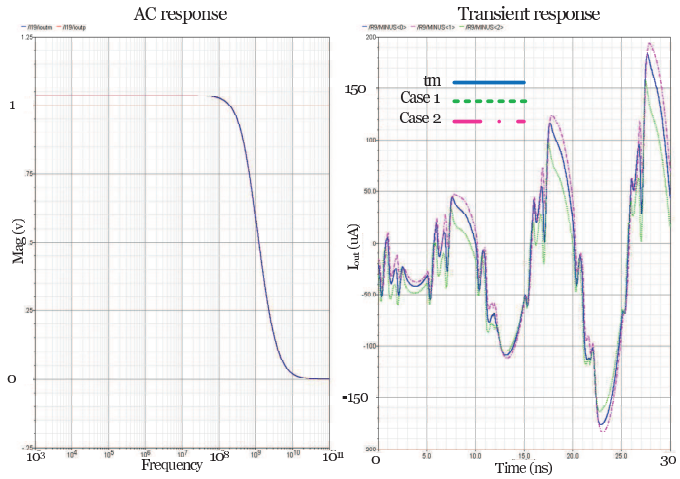

Figure 6.32: AC response (a) and the transient response of the CTOC output.

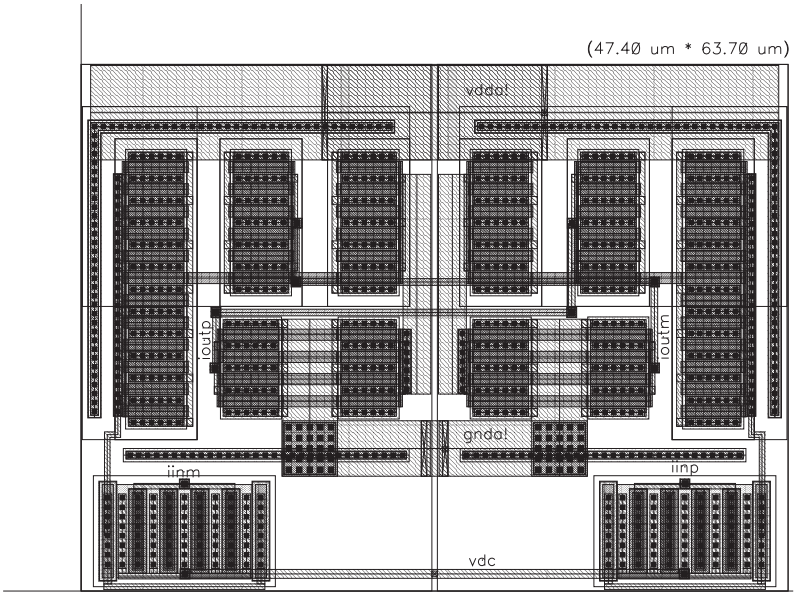

Figure 6.33: Layout of the CTOC circuit.

6.4.4 Amplifier

V_{dc1} and V_{dc2} (figure 6.10) are supplied by the same external source of CTOC to ensure the linearity of the input stage. The trans-impedance gains (R_1 and R_5) are equal to $\frac{\pm 0.25\ V}{\pm 100\ \mu}$. When the gain of the differential stage is equal to 1 ($R_3 = R_4 + R2$), the LSB of the ADC is quite small ($\frac{\pm 0.25\ V}{2^3 - 1}$) and the design of the comparators may face several problems. Therefore, the gain of the differential stage is taken equal to four resulting in a LSB equal to $\frac{\pm 1\ V}{2^3 - 1}$. For this aim, $R_2 = R_4 \cong 2 * R_3$ and the resistors value are chosen to ensure the swing of the differential amplifier. The optimized devices characteristics are listed as follows:

- $V_{dc} = 3\ V$.
- $R_1 = R_3 = R_5 = 2500\Omega$ (rpolyh $W = 5\ \mu m$, $L = 10\ \mu m$), $R_2 = R_4 = 5500\Omega$ (rpolyh $W = 5\ \mu m$, $L = 22\ \mu m$).
- T_1, T_2, T_3, T_4: npn111h5, area=0.8.
- $I_{dc1} = I_{dc2} = I_{dc3} = I_{dc4} = 150\ \mu A$.

The linearity, the transient response and the DC response of the output voltage and the AC response of the circuit are shown in figure 6.34 for typical mean values and the worst cases of the design. Visibly, the worst cases of the design results in DC point and gain variations. Figure 6.35 is the layout of the amplifier circuit. The required chip area is large because of the employed resistors.

6.4.5 Analog to digital converter

6.4.5.1 comparator

Figure 6.36 shows the transient response of the comparators input, threshold voltages and the output of the comparators. In this simulation, the input voltage of the comparators is provided by the amplifier and the amplifier input is a pure sinusoidal current at 100 MHz. Although the size of T_1 and T_4 is chosen as small as possible, the input signal is still affected by parasitic capacitances. The optimized devices characteristics are listed as follows:

- T_1, T_4, $T5$, T_6: $\frac{W}{L} = \frac{11.2\ \mu m}{0.35\ \mu m}$.

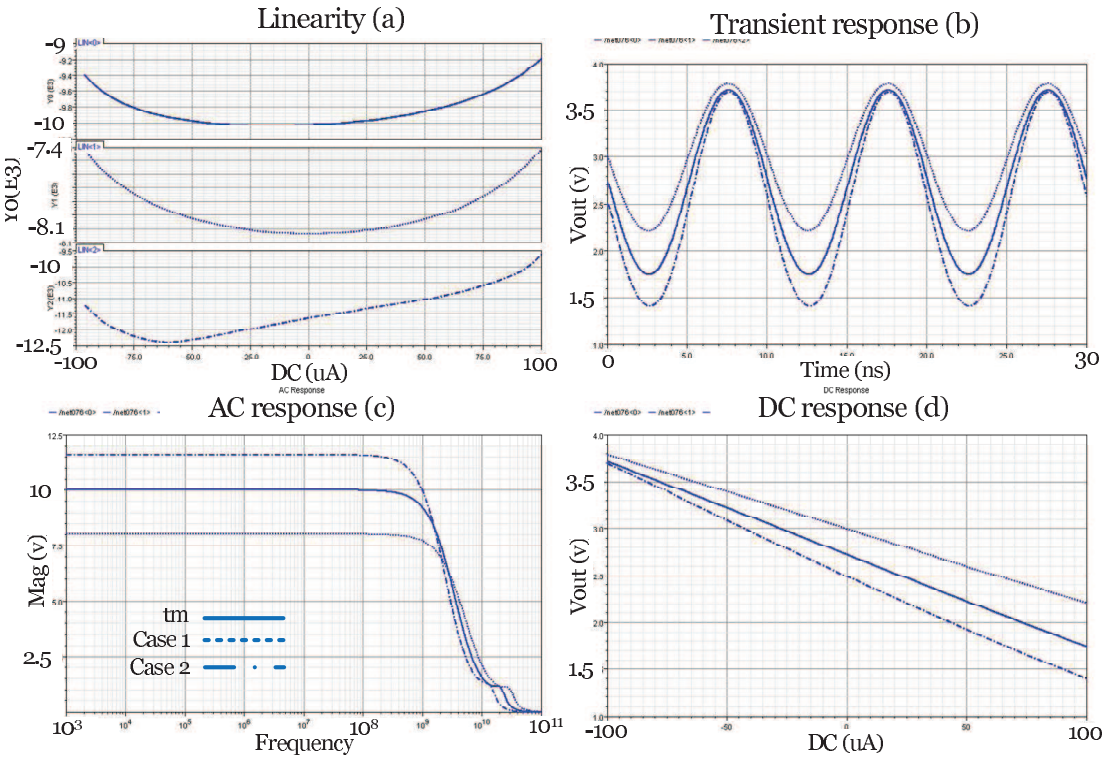

Figure 6.34: Linearity (a), the transient response (b) and the DC response (d) of the output voltage and the AC response (c) of the circuit.

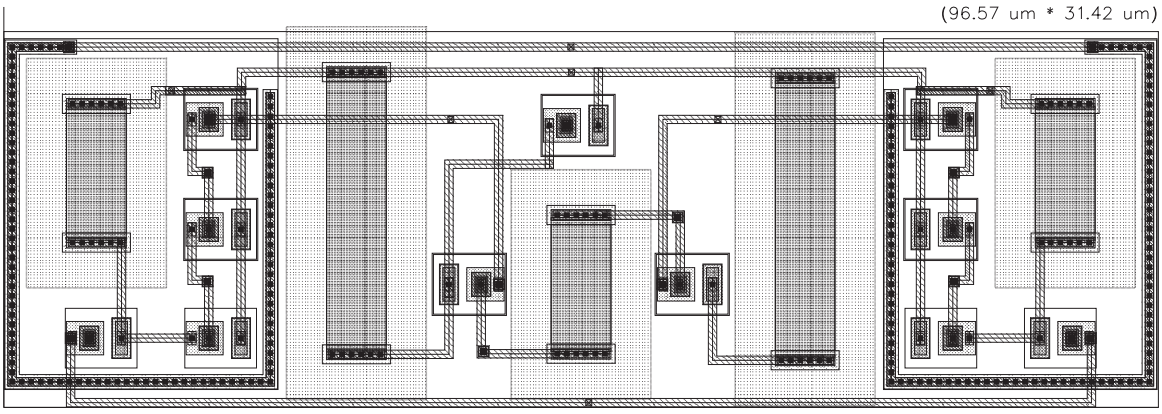

Figure 6.35: Layout of the amplifier circuit.

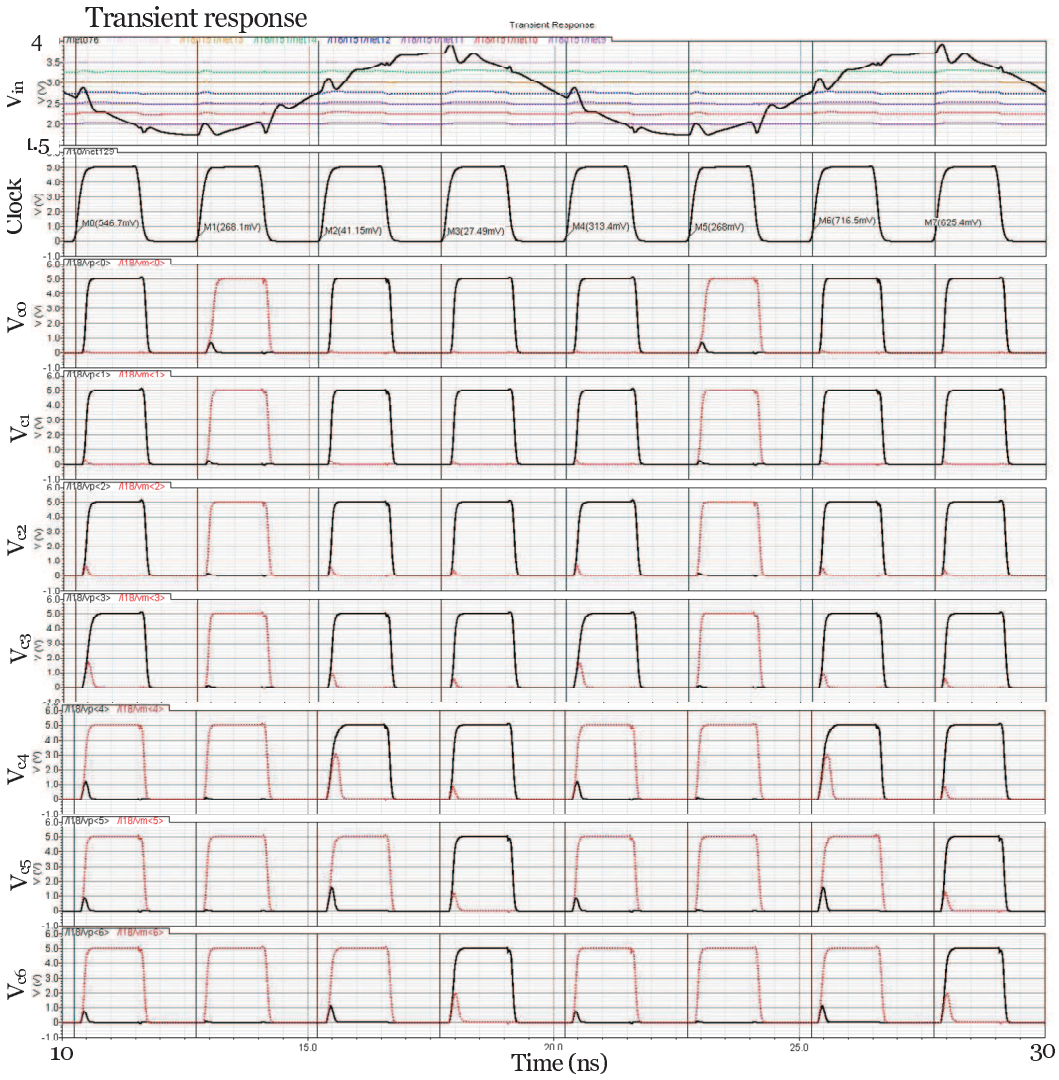

Figure 6.36: Transient response of the comparators input, threshold voltages and the output of the comparators.

- T_2, T_3: $\frac{W}{L} = \frac{2.8\ \mu m}{0.35\ \mu m}$.
- T_7, T_8, $T9$, T_{10}: $\frac{W}{L} = \frac{42\ \mu m}{0.35\ \mu m}$.
- T_{11}, T_{13}: $\frac{W}{L} = \frac{5\ \mu m}{0.35\ \mu m}$.
- T_{12}, T_{14}: $\frac{W}{L} = \frac{1\ \mu m}{0.35\ \mu m}$.

Figure 6.37 is the layout of the comparator circuit. Comparing the required chip area for the comparator circuit with that of other analog components shows the disadvantage of high resolution Flash A/D converters in terms of chip area. Since the current peaks because of the comparators switch function are large, the power supply and the ground of the comparators are separated from the analog and the digital parts.

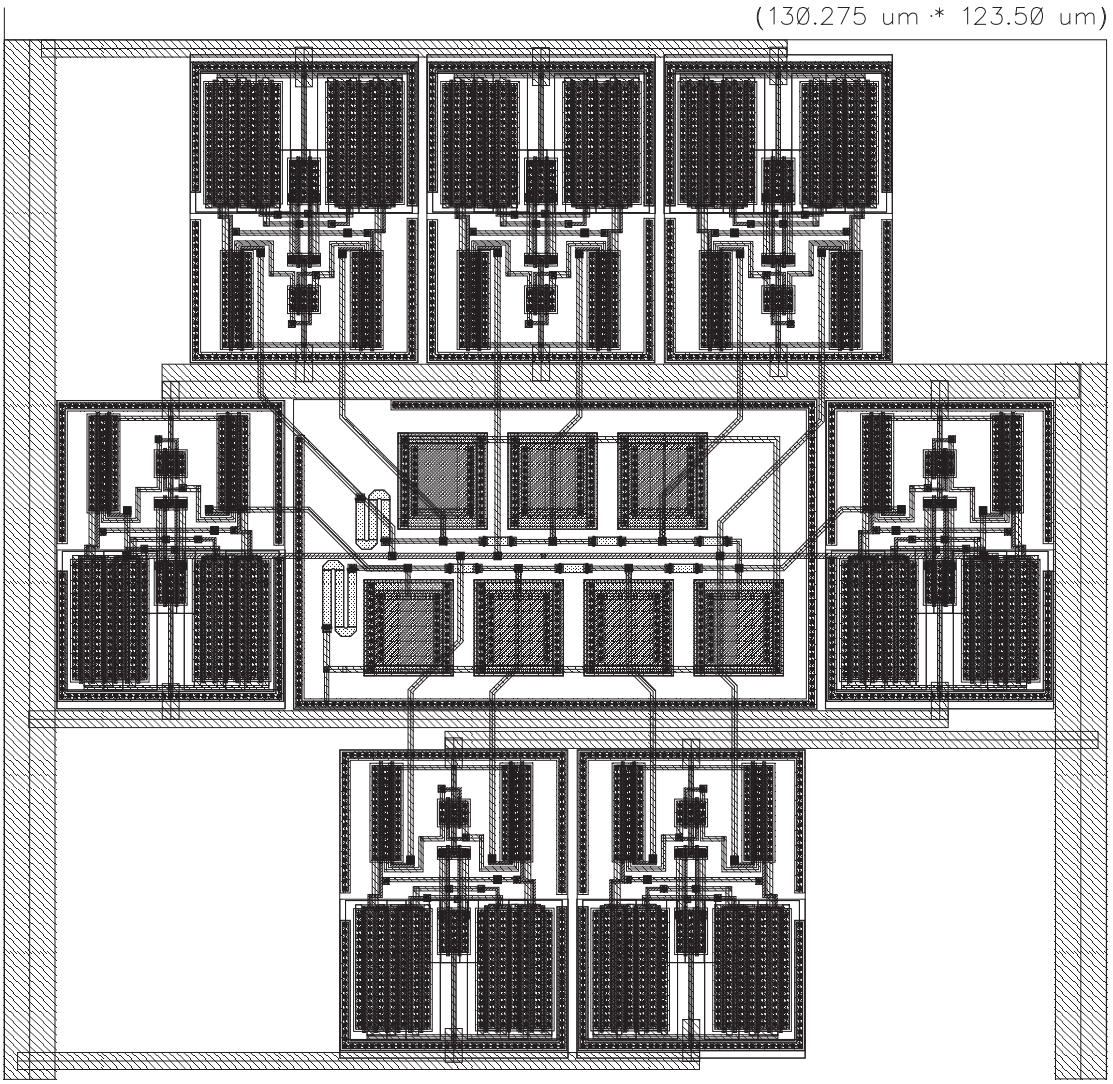

Figure 6.37: Layout of the comparator circuit.

6.4.5.2 Rectifier system

The arrived clock signal, the inputs level and the outputs level of flip-flop$_6$ are shown in figure 6.38. As it is shown, the output signal, compared with the input signal, has a delay equal to $1T_s$. The size of the transistors is chosen as small as possible to reduce the required chip area though the resulting glitches in the output. Note that the size of cells in the digital part is very important because each cell is repeated seven-times. The flip-flop output must pass through a delay cell since the required loop delay is equal to $1.5T_s$. Therefore, glitches will be eliminated by inverter gates of the delay cell. The optimized devices characteristics are listed as follows:

- T_1: $\frac{W}{L} = \frac{11\ \mu m}{0.35\ \mu m}$.
- T_2, T_3, T_6, T_7: $\frac{W}{L} = \frac{3\ \mu m}{0.35\ \mu m}$.
- T_4, T_5: $\frac{W}{L} = \frac{1\ \mu m}{0.35\ \mu m}$.

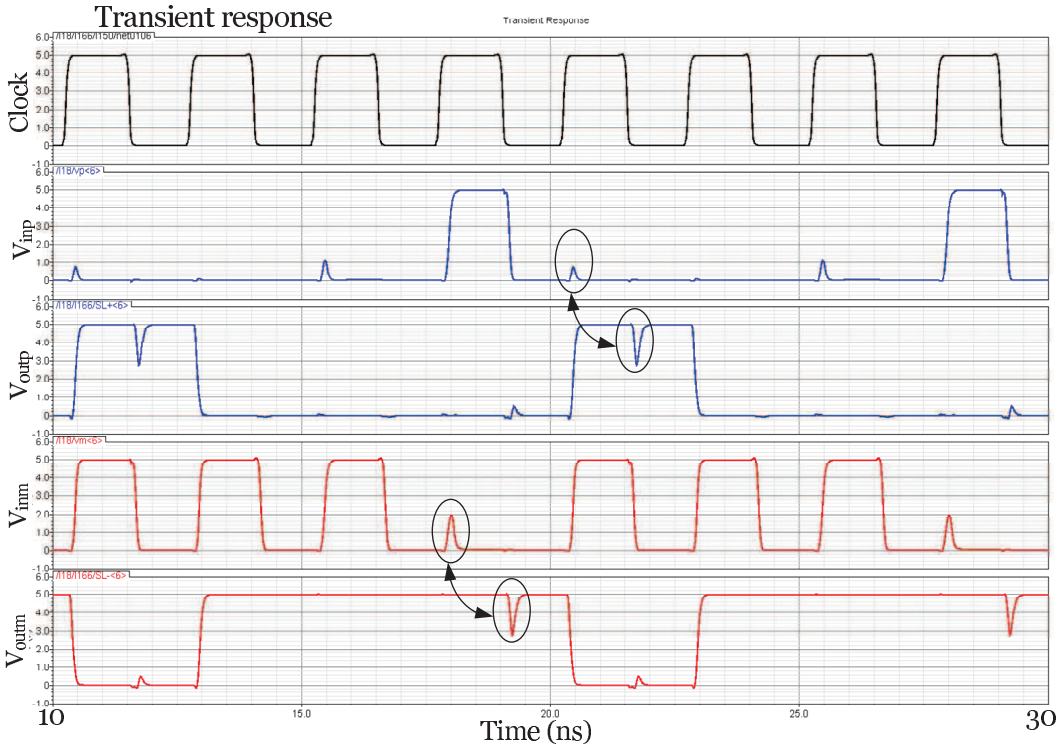

Figure 6.38: Arrived clock signal, the input level and the output level of flip-flop$_6$.

6.4.5.3 Delay

The required modulator loop delay is equal to $1.5T_s$. A portion of this delay ($1T_s$) is provided by the internal delay of the rectifier system. Then an extra delay is required to provide the remained portion ($0.4T_s$). It should be noted that the delay of the analog components in the forward loop is extracted through a transistor-level simulation and is close to $0.1T_s$. Figure 6.39 shows the transient response of the delay input signal (being the flip-flop output signal) and the delay output. Visibly, glitches of the flip-flop output are removed. The optimized devices characteristics are listed as follows:

- T_1, T_3: $\frac{W}{L} = \frac{0.8\ \mu m}{0.8\ \mu m}$.
- T_2, T_4: $\frac{W}{L} = \frac{0.4\ \mu m}{0.8\ \mu m}$.

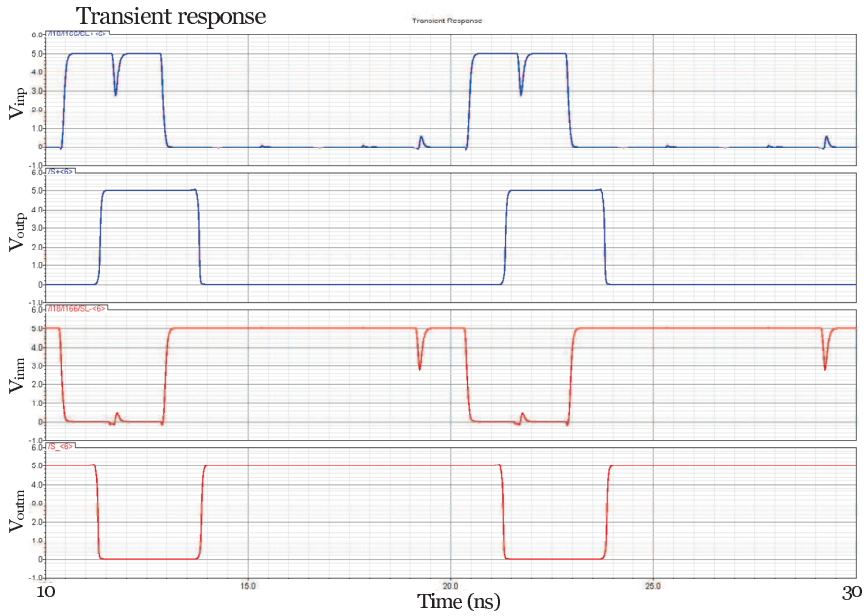

Figure 6.39: Transient response of the delay input signal and the delay output.

Figure 6.40 shows the influence of the worst cases of the design on the ADC performance. In this simulation, the input voltage of the ADC is provided by the amplifier when its input is a pure sinusoidal current at 100 MHz. As it is shown, the amplitude and the DC-offset of the input voltage is affected by the worst cases while the threshold voltages are almost immune. Considering the first branch (V_{in0}), the input signal is not

detected for the first worst case of the design and the ADC output does not change its level. On the other side, the output signal for the typical mean value and the second worst case of the design are detected. However, because of the influence of the second worst case of the design on the delay performance, the ADC output has a larger delay than that of the typical mean values. These issues are not critical for a second-order $\Sigma\Delta$ modulator and may results in resolution loss while for a 6^{th}-order modulator these will almost certainly cause instability issues. Auto-correction methods must forcibly be considered.

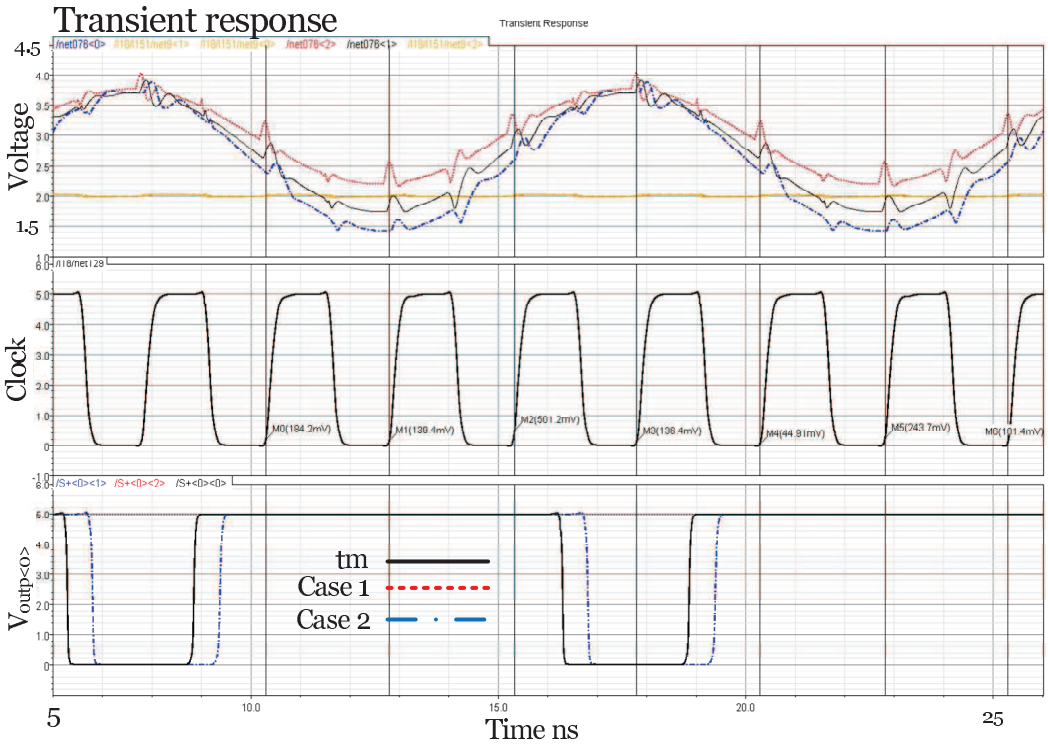

Figure 6.40: Input voltage, the clock signal and the DAC output for typical mean values and the worst cases of the design.

Figure 6.41 is the layout of the digital part of the ADC (being the rectifier system and the delay). The circuit is protected by a guard ring. Moreover, an independent power supply and ground is considered in order to reduce the spread of the clock to the analog part.

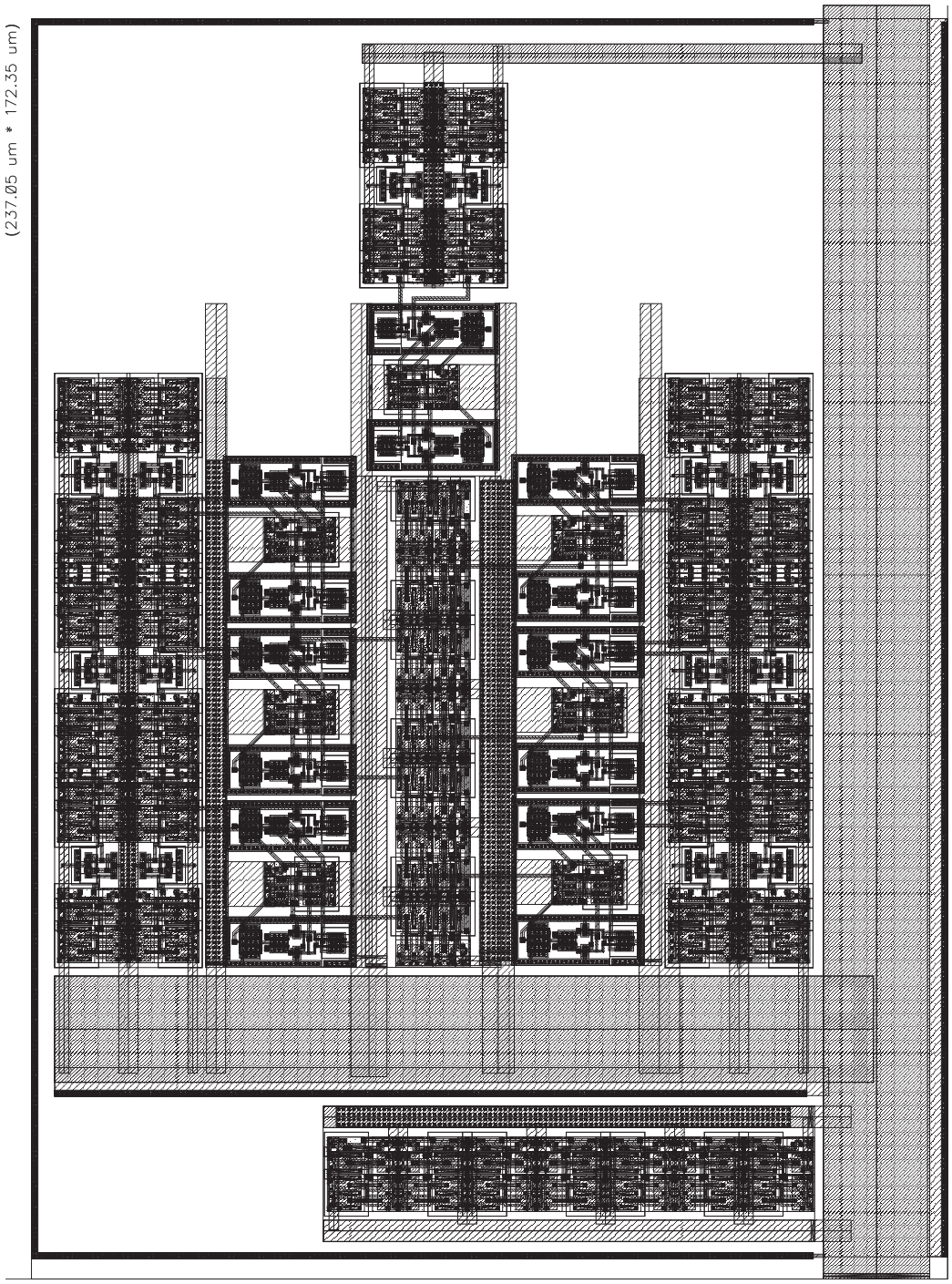

Figure 6.41: Layout of the digital part of the ADC (being the rectifier system and the delay).

6.4.6 Digital to analog converter

The rise and fall time of the output current of the DACs are sensitive to V_{dc1} and V_{dc2} (figure 6.42) while the symmetry between the rise and the fall time is important to eliminate the common-mode distortions in $\Sigma\Delta$ modulator.

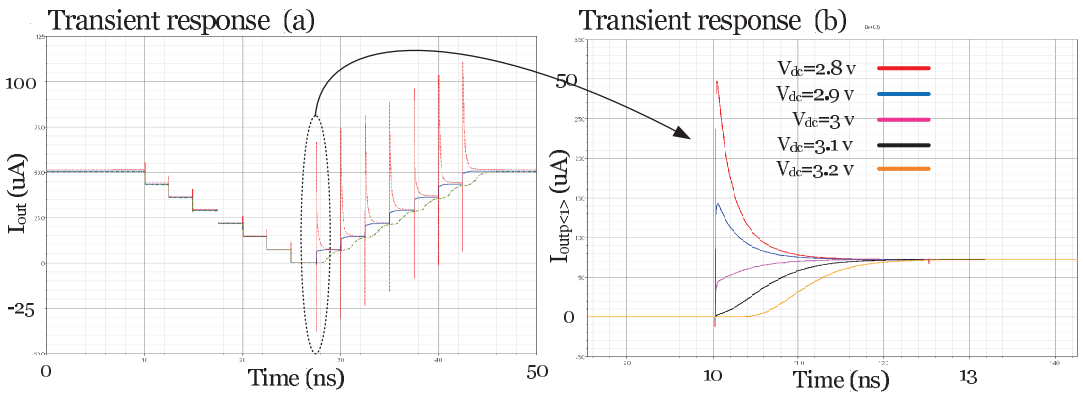

Figure 6.42: Sensitivity of the rise-time of the output current of DAC_2 to V_{dc2}.

The optimized devices characteristics of the DAC_1 are listed as follows:

- $V_{dc1} = 2.8\ V$, $V_{dc2} = 2.71\ V$.
- T_1, T_2, T_3, T_4: $\frac{W}{L} = \frac{8\ \mu m}{1\ \mu m}$.
- $i_{dc1} = 28.57\ \mu A$.

Those of the DAC_2 are also given by:

- $V_{dc1} = 2.8\ V$, $V_{dc2} = 2.97\ \ V$.
- T_1, T_2, T_3, T_4: $\frac{W}{L} = \frac{8\ \mu m}{1\ \mu m}$.
- $i_{dc1} = 7.14\ \mu A$.

They are the same circuits driven by different I_{dc} and bias voltages. The transient responses of them for an input level beginning from [0000000], arriving to [1111111] and coming back to [0000000] are shown in figure 6.43.
Figure 6.44 is the layout of the DAC circuit.

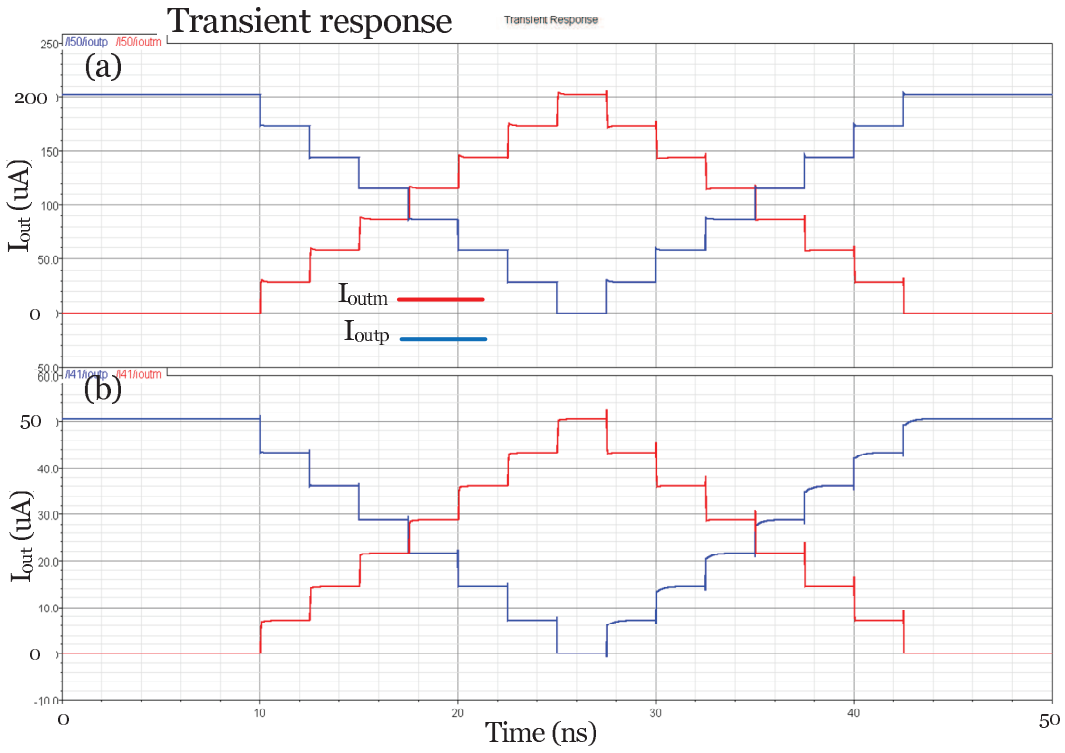

Figure 6.43: Transient response of the DAC_1 output (a) and the DAC_2 output.

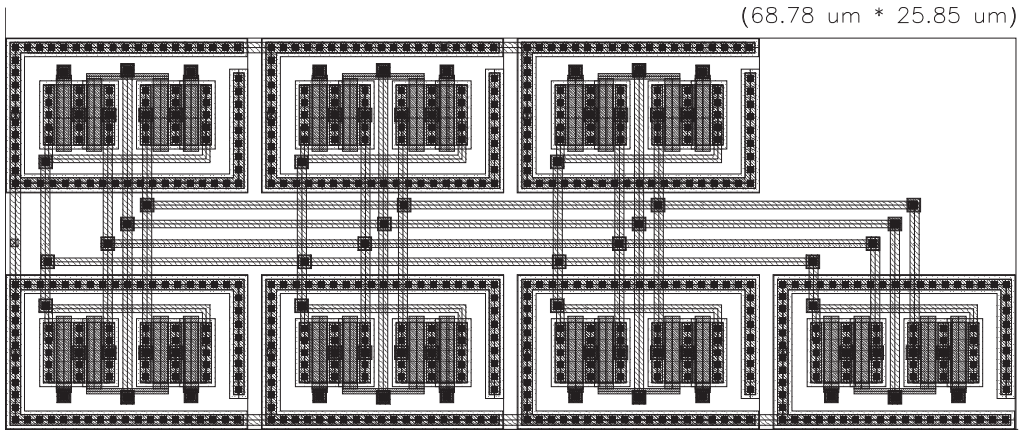

Figure 6.44: Layout of the DAC circuit.

6.4.7 Clock generator

Predictability, the clock circuit is highly sensitive to analog imperfections (figure 6.45). Therefore, V_{dc} is an external voltage to be able to set the clock frequency. The optimized devices characteristics are listed as follows:

- $V_{dc} = 2.26\ V$.
- T_i: $\frac{W}{L} = \frac{3.5\ \mu m}{3.5\ \mu m}$.

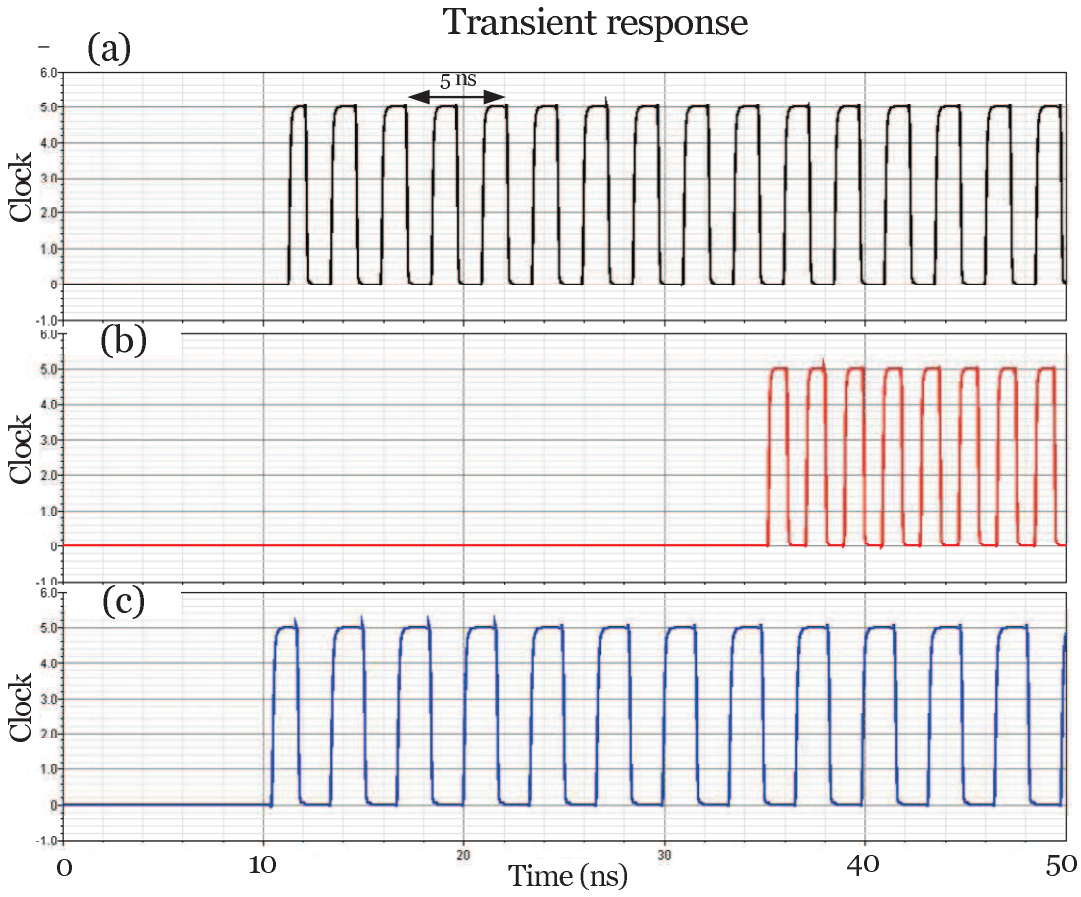

Figure 6.45: Clock generator output for the typical mean values (a), the first worst case of the design (b) and the second one.

Figure 6.46 is the layout of the clock circuit containing the clock generator and the clock tree.

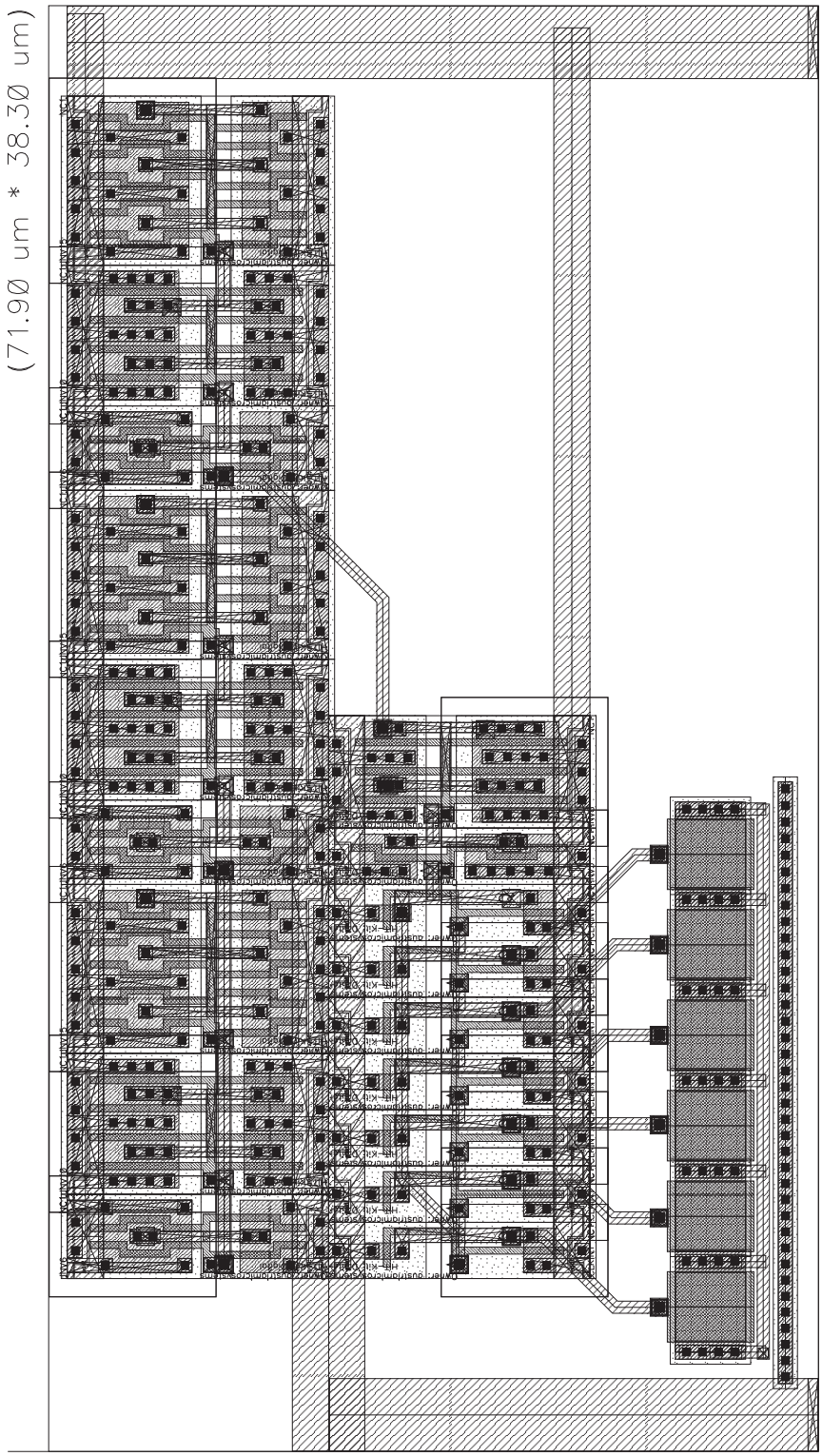

Figure 6.46: Layout of the clock circuit containing the clock generator and the clock tree.

6.4.8 The performance of the second-order ΣΔ modulator

The second-order modulator is simulated in layout-level and figure 6.47 shows the connected analog components in layout-level. As it is shown, the current sources are separated from other components since they are heat sources.

The equivalent electrical model of the LWR (figure 4.7) is used in this simulation. Moreover, the connection between the off-chip power supplies and the LWR with the integrated circuit are provided through the PADs in order to study the influence of their parasitic capacitances. Figure 6.48, figure 6.49 and figure 6.50 show the current or voltage of the important nodes for the typical mean values. The input voltage is a sinusoidal voltage at 100 MHz (figure 6.48.a) and its amplitude is set to $\frac{V_{ref}}{2} = 0.125\ V$. Figure 6.48.b is the output signal of the VTOC circuit. The blue path corresponds to the positive differential signal and the red on corresponds to the negative one.

Figure 6.48.c is the output current of the DAC_1. Although the rise and fall times are smoothed because of parasitic capacitances, the symmetry between I_{outp} and I_{outm} is maintained. Figure 6.48.d is the input current of the CTOV circuit containing the DAC_1 output and the VTOC output. Visibly, this current contains high frequency components. Figure 6.48.e is the driving voltage of the LWR provided by CTOV. The required current by LWR is shown in figure 6.48.f. Because of high frequency components of the drive voltage, the charge and discharge of the anti-resonance cancellation paths result in large current peaks.

Figure 6.49.a is the output current of the DAC_2. Comparison the DAC_1 output with the second one, shows that the performance of the DAC_2 is more sensitive to analog imperfections. Indeed, the DAC_2 is affected by the large current peaks of the LWR. Figure 6.49.b is the CTOC input containing the LWR output current and the DAC_2 output current. The output of the CTOC circuit is shown in figure 6.49.c. The current peaks are almost eliminated. Figure 6.49.d shows that the amplifier is more affected in layout-level simulation by the clock than the transistor-level simulation. The reason is the parasitic capacitances of the layout connections.

The consumed current by the digital part, analog part and the comparators are shown in figure 6.50. Although the current peaks are strong, they will be bounded by anti-shock circuits in a practical circuit to protect metal tracks.

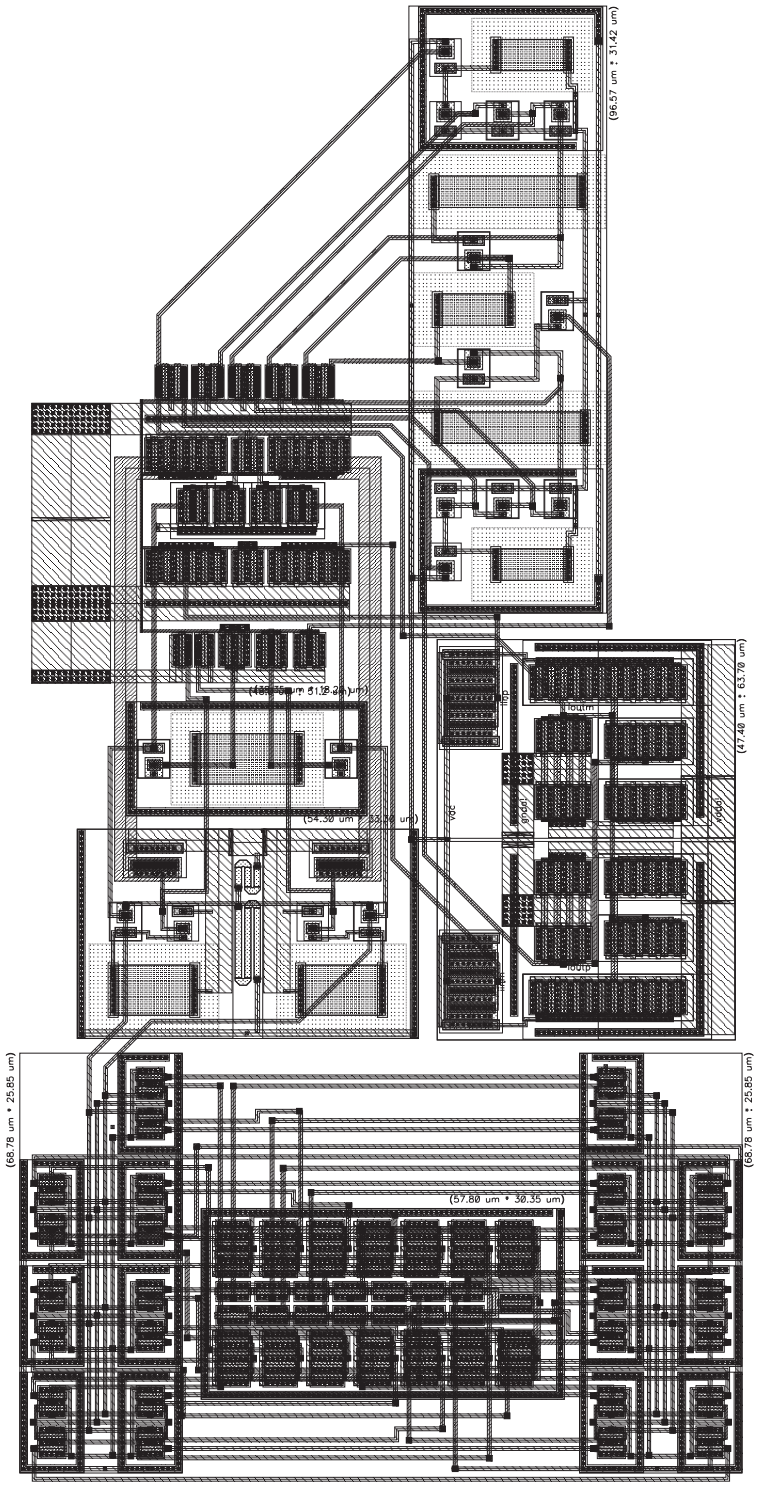

Figure 6.47: Layout of the analog part (including the VTOC, the CTOV, the CTOC, the DAC1, the DAC2 and the current mirrors) of the modulator.

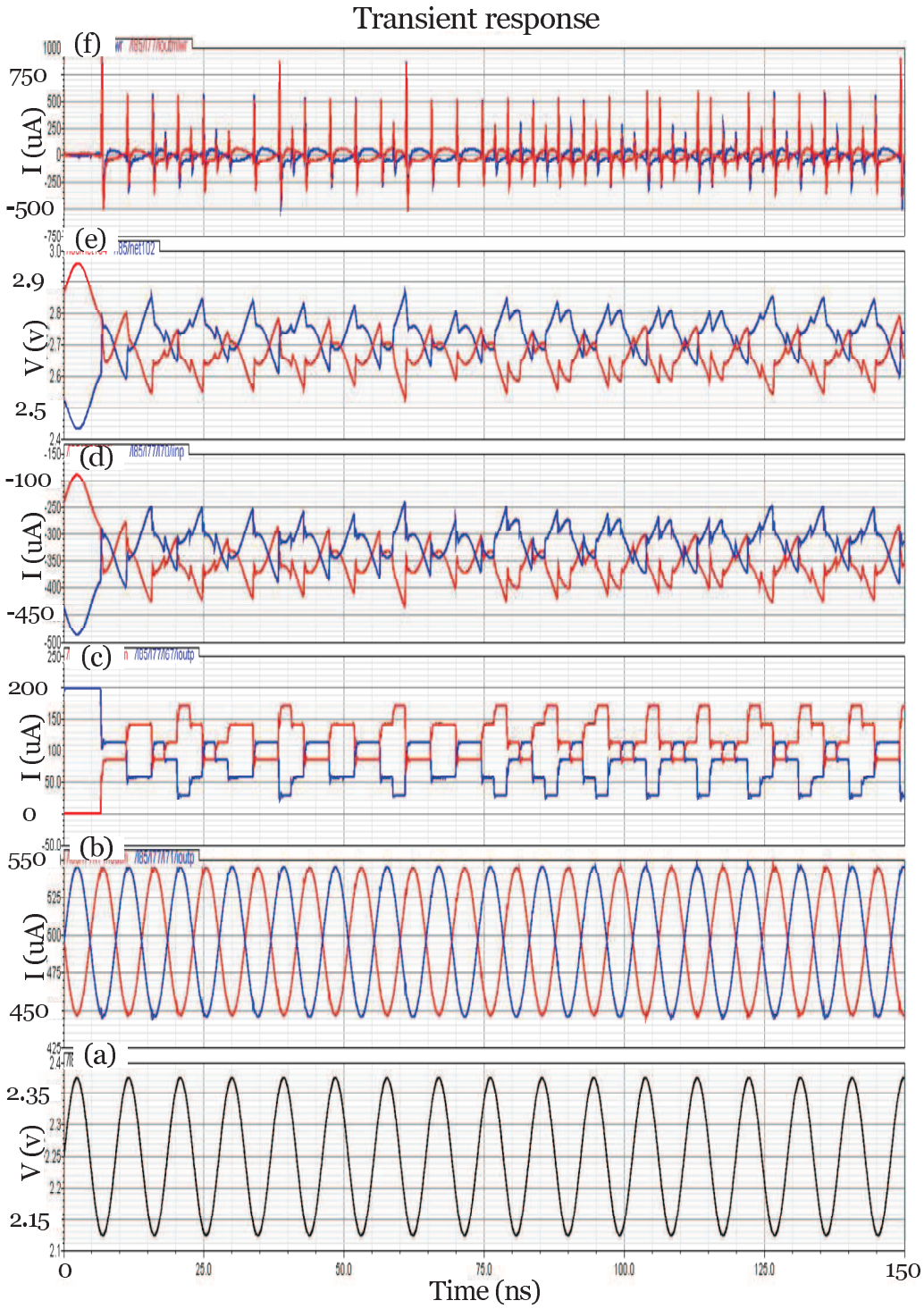

Figure 6.48: Input voltage (a), the VTOC output (b), the first DAC output (c), the CTOV input (d), the CTOV voltage output (e) and the CTOV current output (f) for a layout-level simulation of the second-order ΣΔ modulator. Note that the blue signal corresponds to the positive differential signal and the red on corresponds to the negative one.

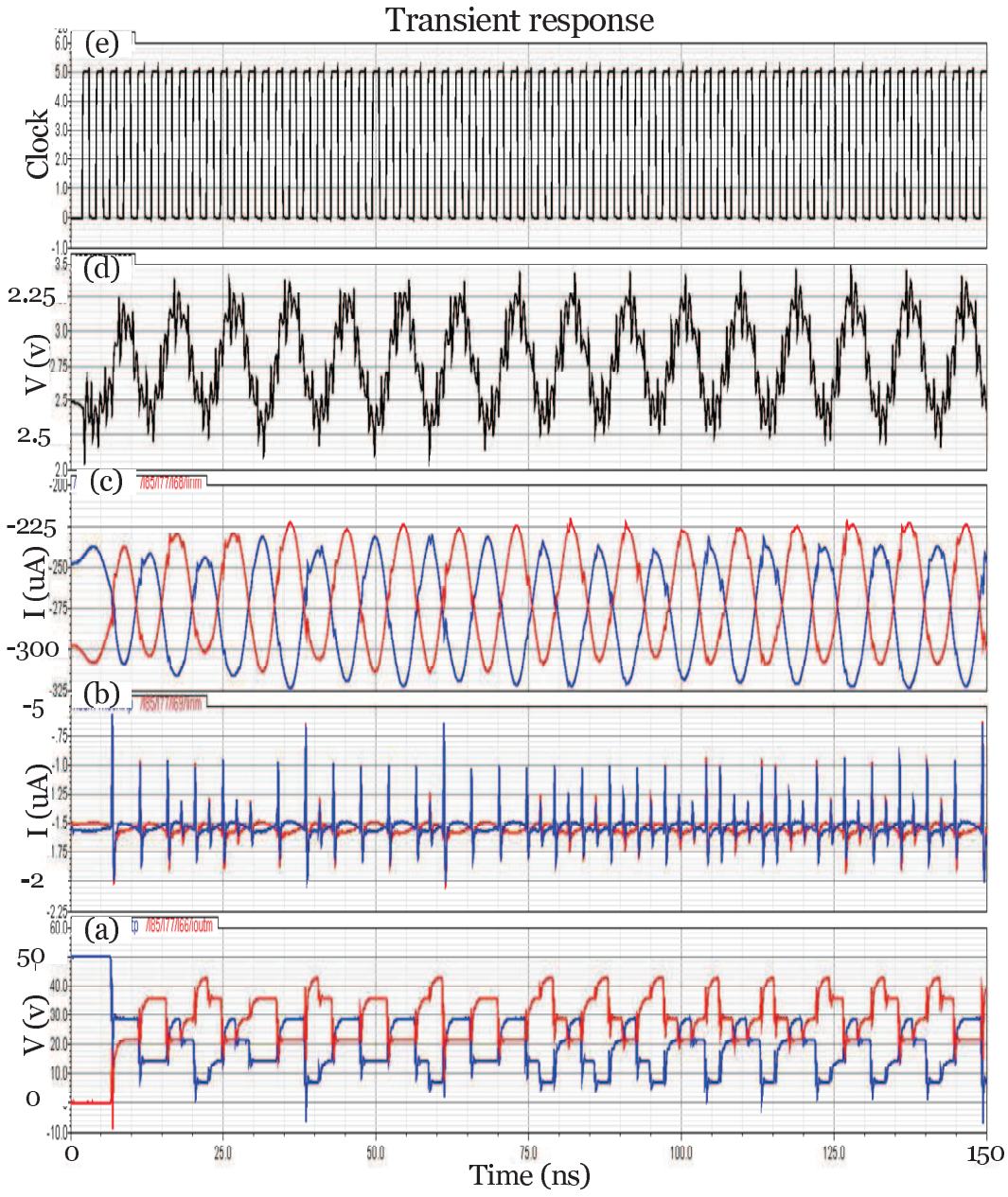

Figure 6.49: Second DAC output (a), the CTOC input (b), the CTOC output (c), the amplifier output (d) and the clock signal (e) for a layout-level simulation of the second-order ΣΔ modulator. Note that the blue signal corresponds to the positive differential signal and the red on corresponds to the negative one.

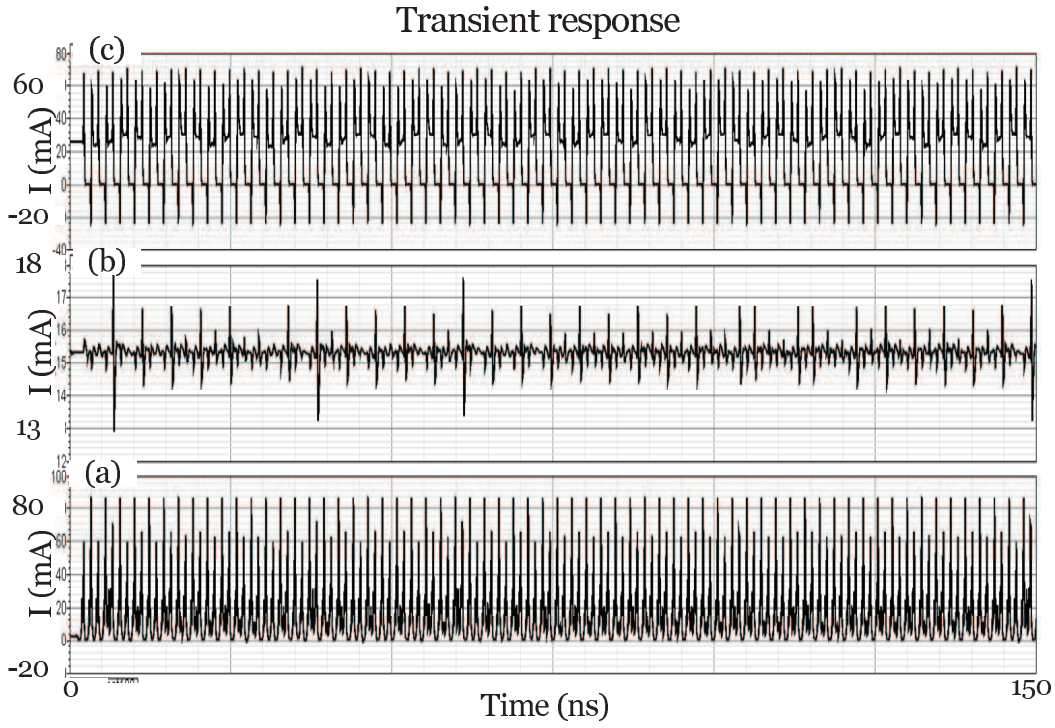

Figure 6.50: Consumed current by the comparators (a), the analog parts (b) and the digital part (c) for a layout-level simulation of the second-order $\Sigma\Delta$ modulator.

The power spectrum density of the modulator output for the typical mean values, the first worst case of the design and the second one are, respectively, shown in figure 6.51.a, figure 6.52.a and figure 6.53.a for 4400 points of simulation. Regarding the sampling frequency, the simulation of the modulator in layout-level is highly time-consumer. The simulation of the modulator for 4400 points takes almost 3 days on the available platform. In order to verify the modulator performance, the output spectrum density of the simulated modulator by CADENCE is compared with the output spectrum density of an ideal modulator simulated by SIMUINK (figure 6.51.b, figure 6.52.b and figure 6.53.b). Although the simulation is done for 4400 points, Only 1100 frequencies are shown for the sake of visibility. The modulator has a good performance for typical mean values while the noise level for the first worst case of the design is significantly larger compared with SIMULINK result. On the other side, a pole appears at $0.32f_s$ for the second worst case of the design which means that the stability of the modulator is reduced because of analog imperfections. Table 6.3 compares the in-band noise of the ideal modulator and the different cases of CADENCE simulation for an OSR equal to 64. Visibly, the objective (satisfying performance in *tm* and maintaining the stability for worst cases) is attained.

Table 6.3: Comparison the in-band noise of the simulated modulator by CADENCE and that of the ideal modulator simulated by SIMUINK for OSR=64.

	SIMULINK	tm	worst case I	worst case II
Noise density (dB)	−60 dB	−56 dB	−52 dB	−47 dB

6.5 Model Extraction

According to the simulation results of a second-order modulator in layout-level, analog imperfections must be seriously taken into account in the design of a 6^{th}-order modulator. The designed components should provide a proper performance to ensure the modulator performance while there is no criterion to verify the suitability of a component expecting the performance of the modulator. In the present work, an optimization method was developed in order to optimize the modifiable parameters accounting analog imperfections. Although this method was tested with simple model of analog

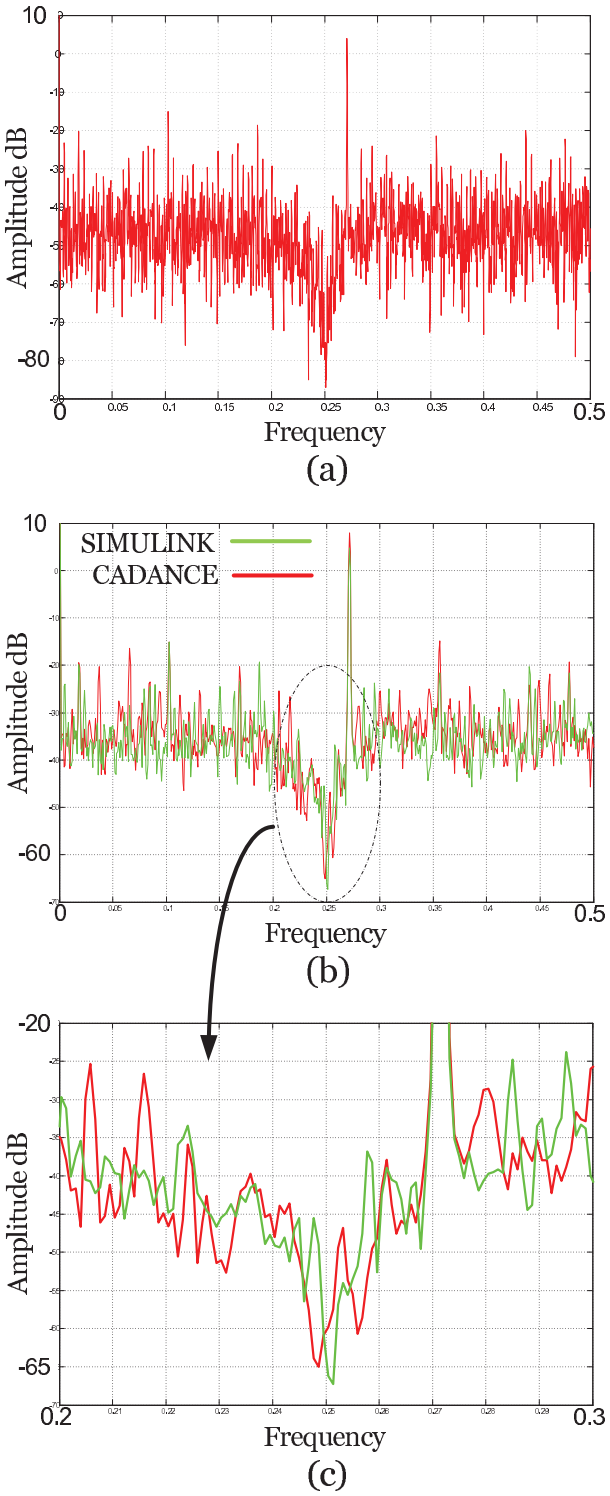

Figure 6.51: Power spectrum density of the modulator output, simulated in layout-level, for 4400 points of the simulation (a) compared with an ideal modulator simulated by SIMULINK, where 1100 points are illustrated (b), for the typical mean value.

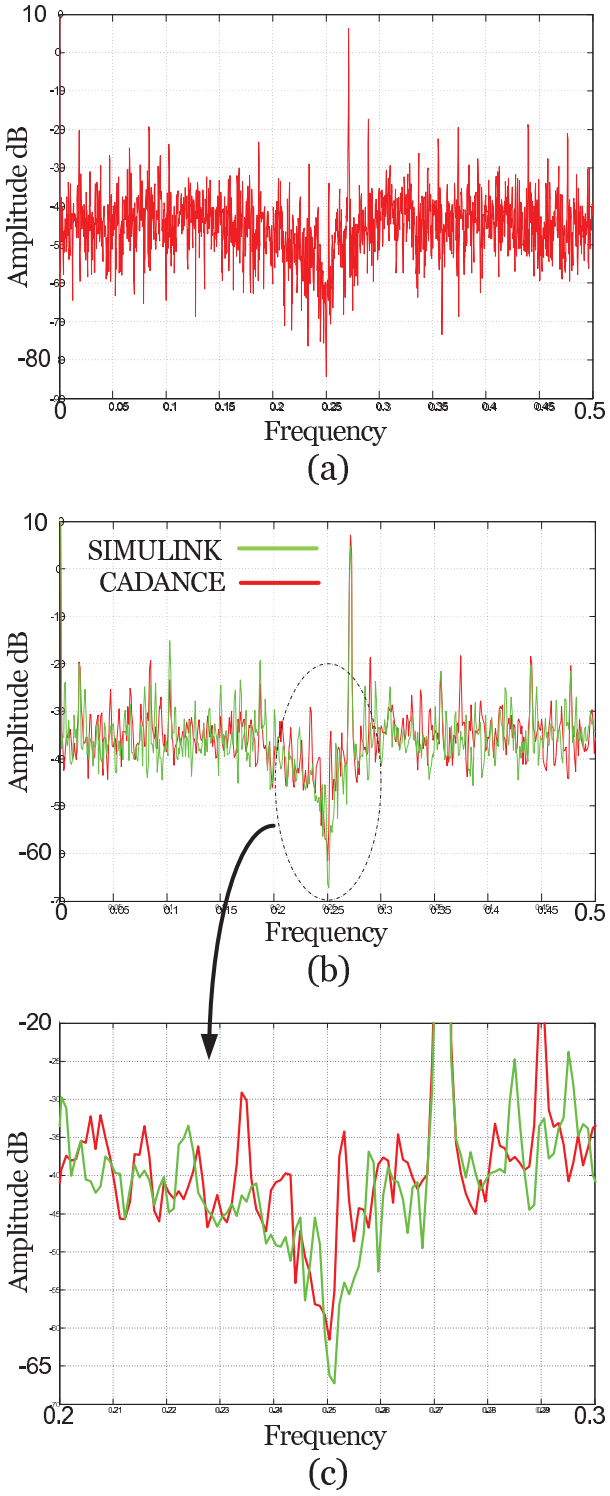

Figure 6.52: Power spectrum density of the modulator output, simulated in layout-level, for 4400 points of the simulation (a)compared with an ideal modulator simulated by SIMULINK, where 1100 points are illustrated (b), for the first worst case of the design.

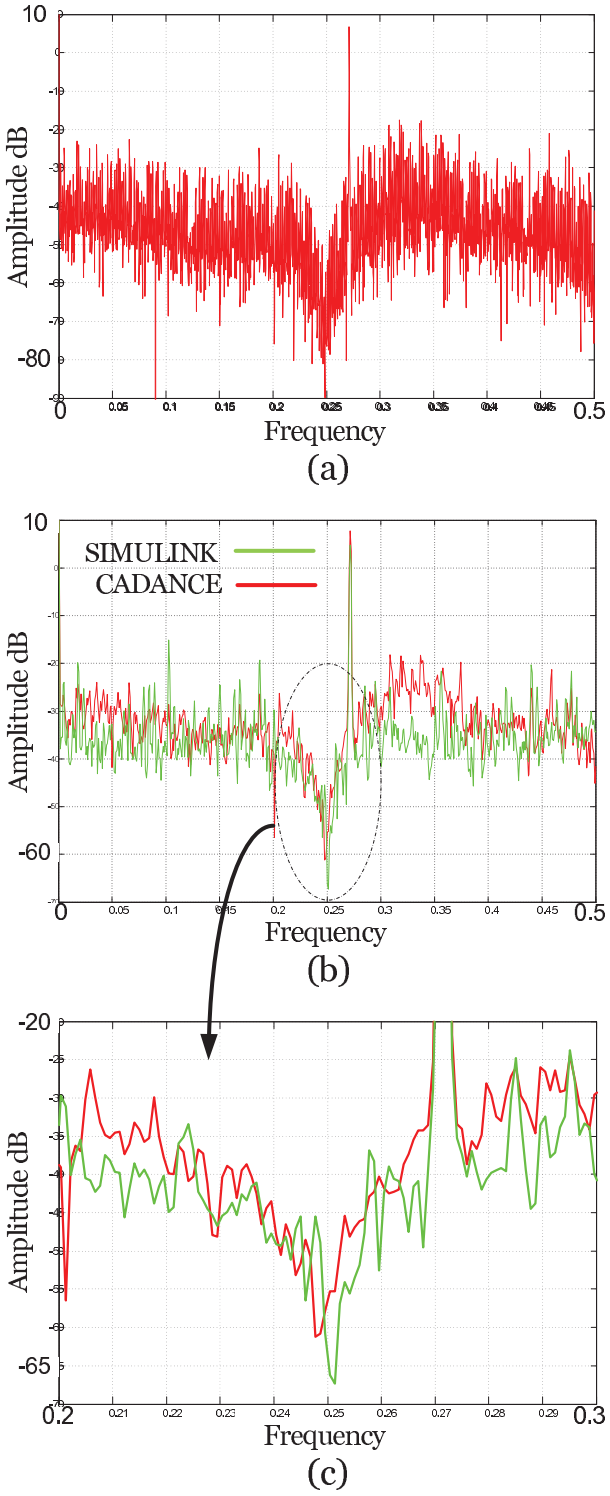

Figure 6.53: Power spectrum density of the modulator output, simulated in layout-level, for 4400 points of the simulation (a) compared with an ideal modulator simulated by SIMULINK, where 1100 points are illustrated(b), for the second worst case of the design.

components, system-level models of real components extracted from a transistor-level simulation are necessary to ensure the reliability of the designed modulator. Then, the proposed method gets as input the system-level models and gives as output the optimized modifiable parameters. The main advantage consists in designing a reliable modulator with minimum constraints on electronic design.

The model extraction was the subject of an internship done by Tugui [153] in parallel with the present work. A MATLAB utility has been developed to extract automatically electrical models of analog components through a transistor-level simulation in CADENCE. The transfer function, the input impedance and the output impedance of components have been extracted through an AC simulation and the offset voltages and the non-linearity coefficients have been extracted through a DC simulation. The order of the resulting global filter transfer function ($G(s)$) is high (up to 30 or 40) and it contains low and high frequency poles and zeros. Since a CT to DT transfer is used to calculate the stability margin, the order of the global filter transfer function must be reduced. This can be done by removing the poles and zeros with a much higher frequency compared with the sampling frequency. The difference between the numerator and the denominator of the global filter must be respected after removing the high frequency poles and zeros.

These solutions were employed in [154] to design a 6^{th}-order $\Sigma\Delta$ modulator working at $f_c = 0.25 f_s$ in transistor-level for typical mean values. The results have been approved the correctness of the proposed design methodology.

6.6 Conclusion

The required components in order to implement the proposed topology were studied. Also, proper schematics compatible with AMS Bi-CMOS 0.35 μm technology have been proposed. Of available technology kits, AMS Bi-CMOS 0.35 μm technology was chosen because it offers npn BJT transistors. This sort of transistors was indispensable to design low impedance connections by common-collector or common-base arranges. However, the power consumption of these techniques is the main disadvantage.

Since the practical performance of LWRs is unknown for us, the design of a second-order modulator working at $f_c = 0.25 f_s$ has been envisaged to benchmark the solutions.

This was also gave us the opportunity to verify the performance of the proposed components in a $\Sigma\Delta$ modulator loop. Once the efficiency of the proposed solutions in transistor-level, layout-level and a fabricated circuit is approved, the design of a 6^{th}-order modulator can be envisaged.

The design of the second-order modulator was done in layout-level. The major issues have been concerned the differential-mode functionality of layed out components and the deviation of the characteristics of the components in the worst cases of the design from their nominal characteristics. Since in the context of a benchmark circuit, there was no intention of designing auto-correction methods, strict rules on layout design were considered. Moreover, an external current reference was used to reduce the DC point variation of analog components. Respecting the proposed considerations was very important because if the fabricate circuit is instable, there is no possibility to recover the performance by external tuning.

The results of the simulation in layout-level have shown the efficiency of the proposed solutions for typical mean values while the modulator performance was slightly deteriorated for the worst cases of the design. Although for a second-order modulator the deviation of the characteristics of the components in the worst cases of the design from their nominal value was not critical, this makes a 6^{th}-order $\Sigma\Delta$ modulator almost certainly instable. This is the main drawback of electronic design of high-order modulators.

7

Conclusions and perspectives

7.1 Conclusions

The presented work was about the design of high-order continuous-time band-pass sigma-delta modulators for parallel A/D converters.
Parallelism is one of the possible solutions to increase the ADC bandwidth without degrading its performance. Although various techniques exist to implement a parallel system, the EFBD solution has been chosen because of its low sensitivity to analog imperfections compared with other counterparts. Studying the requirements of an EFBD system resulted in extracting the specifications of the required $\Sigma\Delta$ modulators, especially in terms of resolution, chip area and power consumption.

It was shown that a 6^{th}-order single-stage $\Sigma\Delta$ modulator employing a 3-bits quantizer is theoretically able to provide the required resolution (typically between 12 and 16 bits depending on the communication standards). An OSR equal to 64 has been chosen to make a compromise between resolution and the required number of modulators to cover the frequency band of the EFBD ($0.2f_s < f < 0.3f_s$ in the presented work). Continuous-time techniques are indispensable to attain the required operational frequencies although they are highly sensitive to analog imperfections. A proper methodology of design of high-order CT modulators was proposed in order to establish a robust stability regime as well as maintaining the resolution of the modulator.

A new topology based on weighted feedforward techniques offering an adequate control of the position of the NTF poles has been proposed. Moreover, extra signal paths has been added to the topology in order to achieve a filtering-STF close to the

modulator central frequency. This results in increasing the input dynamic range of the modulator. By integrating the simple model of analog imperfections in MATLAB environment, the sensitivity of the proposed topology to analog imperfections has been studied. The results have approved that a simple synthesis of the global filter transfer function, which has been found through its DT counterpart, is not reliable in practice.

An optimization method on the modifiable parameters of the proposed topology was developed in order to recover the performance of the modulator accounting analog imperfections. The system-level models of the analog components, extracted from a transistor-level simulation, is required to ensure the performance of the fabricated modulator. A MTLAB tool was developed during an internship, in parallel with the presented work, for this aim. Then, the optimization tool gets, as input, the system-level model of the analog components and gives, as output, the optimized value of the modifiable parameters. Major advantages of the proposed method include the reliability of the designed modulator with minimum constraints on the electronic design.

It has been also shown that in the context of classical wide-band converters, a large Q-factor is required to ensure the modulator performance. For an given OSR equal to 64, the optimal Q-factor is close to 100. Moreover, the resonance frequency of the used resonator must be as immune as possible to temperature variations and manufacturing process in order to avoid resolution losses. Various sorts of resonators, including Gm-C resonators, Gm-LC resonators, MEMS, SAW resonators, BAW resonators and LWRs have been studied. Of all these solutions, LWRs are the only one able to provide large Q-factors and to work in the band of interest of the presented work with no integration issue. However the parasitic capacitance resulting in anti-resonance, and low impedance connections to ensure the resonator performance, are the main obstacles. A proper electronic control circuit based on differential-mode was proposed to overcome the problems.

Finally, the required analog components of the proposed topology has been designed in transistor-level by AMS Bi-CMOS 0.35 μm technology kit. This technology has been chosen because of the existence of npn BJT transistors. Indeed, they ease the design of low impedance connections. A second-order modulator working at $f_c = 0.25 f_s$ has been chosen as a benchmark in order to verify the compatibility of the proposed solutions with a $\Sigma\Delta$ modulator loop. The design was done in layout-level and the simulations were done for typical mean values and the worst cases of the design. The results have

been approved the correctness of the proposed solutions. However, auto-correction methods must be used to make the performance of the components as immune as possible to the worst cases of design. Although for a second-order modulator the deviation of the characteristics of the components in worst cases of the design from their nominal value was not critical, this makes a 6^{th}-order $\Sigma\Delta$ modulator becomes almost certainly instable. This is the main drawback of electronic design of high-order modulators.

7.2 Perspectives

The proposed methodology of design of high-order modulators has been tested for a second-order modulator designed in layout-level in the presented work and a 6^{th}-order modulator designed in transistor-level in [154] where both of them work at $f_c = 0.25 f_s$. Although the results shows that a proper platform has developed in the presented work, several issues remain to overcome in order to implement an EFBD system employing 6^{th}-order modulators.

First of all is the issues of LWRs. The available piezo-electric resonators are capable of performing large Q-factors while the required Q-factor for large-band modulators is around 100. A study on new structures of LAWRs and high-loss piezo-electric materials must be done to design a convenient resonator.

The second issue concerns the choice of a proper technology. Although low impedance connections have been obtained by common-collector or common-base arranges, the power consumption of these techniques is extremely large. The characteristics of the integration technology should permit the implementation of feedback techniques in order to reduce the impedance of connections. Moreover, the integration technology must be compatible with the deposition of piezo-electric materials in order to implement a monolithic circuit.

The deviation of the characteristic of the analog components in the worst cases of design from their nominal value is the third issue. These deviations are very large. Although the stability of the modulator may be remained in the worst cases of the design by the optimization method, the performance is surely deteriorated. Auto-correction methods should be considered.

The last issue concerns the optimization method. In the presented method, the modifiable parameters are gain coefficients found through the system-level model of analog components. The integration of the optimized parameters in transistor-level result in modifying the characteristics of the corresponding analog components. This may result in performance degradation if the modifications are large. An alternative solution consists in optimizing the components parameters (such as bias currents and resistors) instead of components characteristics (such as gain and input or output impedance).

Once the design of a 6^{th}-order modulator is accomplished, the design of an EFBD system can be envisaged as a long term perspective.

Appendix A

Multi Stage closed Loop Modulators (MSCL) was introduced for the first time in [41]. Low-order (second-order or fourth-order) modulators are put in cascade to achieve a high-order modulator. Figure A.1 shows a typical second-order MSCL structure employing two low-order modulator ($\Sigma\Delta_1$ and $\Sigma\Delta_2$). The advantage consists in conserving the stability characteristic of the employed low-order modulator. The feedback path, connecting the output to the input, must be calibrated to ensure the global performance.

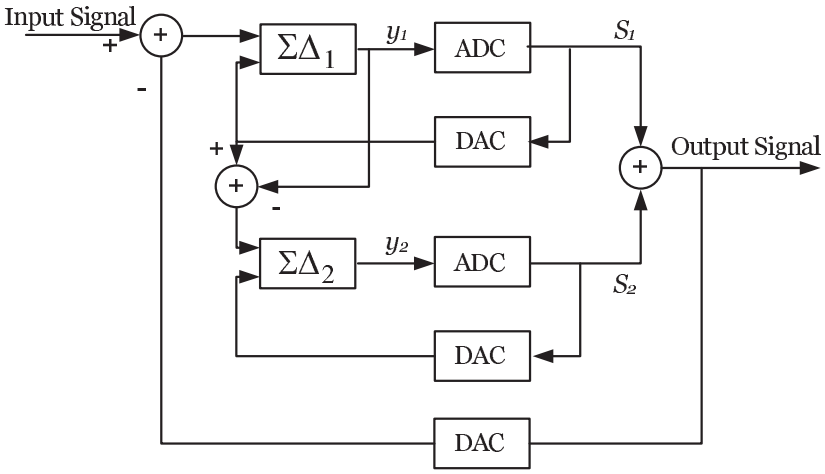

Figure A.1: A second-order MSCL structure.

The equivalent topology of a DT MSCL structure is shown in figure A.2 where $F(z)$ is given by:

$$F(z) = \prod_{j=1}^{n}(1 + c_j\hat{H}_j(z)) - 1. \tag{A.1}$$

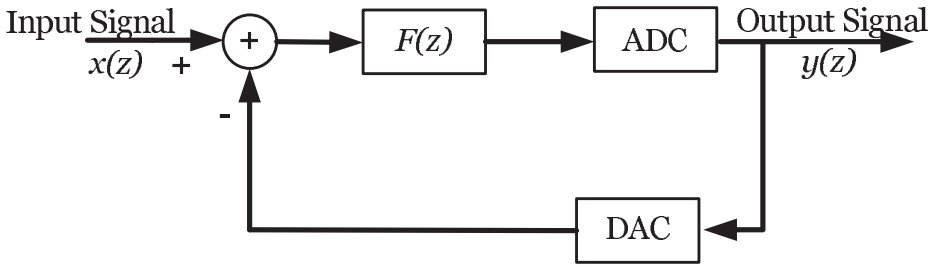

Figure A.2: Equivalent model of a DT MSCL topology.

$\hat{H}_j(z)$ is the transfer function of a band-pass resonator in z domain given by:

$$\hat{H}_j(z) = \frac{A_j(z)}{B_j(z)}. \tag{A.2}$$

Through the linear model of the quantizer the system equation of the equivalent model (figure A.2) is expressed by:

$$y(z) = x(z) + e_n(z) \prod_{j=1}^{n} \mathrm{NTF}_j(z), \tag{A.3}$$

where $\mathrm{NTF}_j(z)$ is the noise transfer function of the employed low-order modulators given by:

$$\mathrm{NTF}_j(z) = \frac{1}{1 + c_j \hat{H}_j(z)}. \tag{A.4}$$

$e_n(z)$ is the quantization noise of the last low-order modulator and that of other modulators are eliminated when the feedback is correctly calibrated. As a result, the STF of a MSCL structure is an all-pass filter with a gain equal to 1 and its NTF is defined as follows:

$$\mathrm{NTF}(z) = \prod_{j=1}^{n} \mathrm{NTF}_j(z). \tag{A.5}$$

A.1 The modulus of the NTF of a 6^{th}-order MSCL employing band-pass resonators with infinite Q-factors

The transfer function of a band-pass resonator with an infinite Q-factor in z domain is given by:

$$\hat{H}_j(z) = \frac{A_j(z)}{B_j(z)} = \frac{\alpha p_j z^{-1} - z^{-2}}{1 - p_j z^{-1} + z^{-2}}. \tag{A.6}$$

The poles of $\hat{H}_j(z)$ are equal to $[e^{j2\pi f_{rj}} \quad e^{-j2\pi f_{rj}}]$ and p_j is defined by:

$$p_j = 2\cos(\frac{2\pi f_{rj}}{f_s}). \tag{A.7}$$

For a second-order modulator, the resonator resonance frequency (f_r) corresponds to the modulator central frequency (f_c). Moreover, f_s is the modulator sampling frequency. In [41], it is demonstrated that the optimal value of α is equal to 0.5 for a modulator central frequencies close to $0.25f_s$. It is also shown that the c_j parameters have a large influence on the modulator stability and must be optimized to increase the stability margin. The denominator of $\hat{H}_j(z)$ can be reformulated as follows:

$$\begin{aligned} B_j(z) &= 1 - p_j z^{-1} + z^{-2} \\ &= z^{-1}(z - p_j + z^{-1}) \\ &= z^{-1}(2\cos(2\pi f) - \cos(2\pi f_{rj})) \\ &= 4z^{-1}\sin(\pi(f + f_{rj}))\sin(\pi(f - f_{rj})). \end{aligned} \tag{A.8}$$

Through the first order approximation around the central frequency, $B_j(z)$ may be approximated by:

$$B_j(z) \approx 4z^{-1}\sin(2\pi f_{rj})(f - f_{rj}). \tag{A.9}$$

$A_j(z)$ can be calculated by using the same method:

$$A_j(z) \approx \sin^(2\pi f_{rj}). \tag{A.10}$$

Assuming that the bandwidth of the employed low-order modulators is sufficiently narrow, $B_j(z)$ tends toward zero for the frequencies close to the modulator central frequency. As a result, the modulus of the NTF_j (equation A.4) may be approximated by:

$$|\text{NTF}_j(z)|^2 \approx \frac{|B_j(z)|^2}{|c_j A_j(z)|^2} = (\frac{4\pi}{c_j})^2(f - f_{rj})^2. \tag{A.11}$$

Finally, the modulus of the NTF of a 6^{th}-order MSCL employing band-pass resonators with an infinite Q-factor is equal to:

$$\mathrm{NTF}(z) = \prod_{j=1}^{n} (\frac{4\pi}{c_j})^2 (f - f_{rj})^2. \tag{A.12}$$

A.2 The modulus of the NTF of a 6^{th}-order MSCL employing band-pass resonators with finite Q-factors

The corresponding band-pass resonator transfer function in s domain to the band-pass resonator transfer function in z domain, given by equation A.6, is expressed by:

$$H(s) = \frac{A(s)}{B(s)} = \frac{\alpha s + a}{(s - s_1)(s - s_2)} = \frac{\alpha s + a}{s^2 + (2\pi f_{rj})^2} = \frac{\alpha s + a}{s^2 + (\omega_{rj})^2}. \tag{A.13}$$

Indeed, $H(s)$ is the transfer function of a band-pass resonator with an infinite Q-factor with a constant term in the numerator (a). Such a resonator does not exist in practice. The transfer function of a practical band-pass resonator in s domain is as follows:

$$H(s) = \frac{\alpha s + a}{s^2 + \frac{\omega_{rj}}{Q} + (\omega_{rj})^2}. \tag{A.14}$$

Considering the hypotheses of pole conservation, the numerator of the corresponding transfer function in z domain to the practical $H(s)$ is same as that of equation A.10. On the other side, its denominator changes and can be calculated as follows:

$$\begin{aligned} B_j(z) &= (z - e^{s_1 T_s})(z - e^{s_2 T_s}) \\ &= (z - e^{\frac{j\omega_{rj}\sqrt{4Q^2-1} - \omega_{rj}}{2Q}})(z - e^{\frac{-j\omega_{rj}\sqrt{4Q^2-1} - \omega_{rj}}{2Q}}) \\ &= z^2 - e^{\frac{-\omega_{rj}}{2Q}} (2\cos(\frac{\omega_{rj}\sqrt{4Q^2-1}}{2Q}))z + e^{\frac{-\omega_{rj}}{2Q}}. \end{aligned} \tag{A.15}$$

If the resonator Q-factor is sufficiently large, $B_j(z)$ can be approximated by:

$$B_j(z) \approx z^2 - p_j(1 - \frac{\omega_{rj}}{2Q})z + (1 - \frac{\omega_{rj}}{2Q}). \tag{A.16}$$

Then, the resonator transfer function of a band-pass resonator with a finite Q-factor in z domain may be approximated by:

$$\hat{H}_j(z) = \frac{0.5 p_j z^{-1} - z^{-2}}{1 - p_j(1 - \frac{\pi f_{rj}}{Q_j})z^{-1} + (1 - \frac{2\pi f_{rj}}{Q_j})z^{-2}}. \tag{A.17}$$

Note that the optimal value of α equal to 0.5 is applied. When the Q-factor is sufficiently large, $B_j(z)$ tends toward zero for the frequencies close to the modulator central frequency and is negligible compared with $A_j(z)$. Then, the NTF_j can be approximated by:

$$\mathrm{NTF}_j(z) = \frac{B_j(z)}{c_j A_j(z)}. \tag{A.18}$$

The numerator of the $\mathrm{NTF}_j(z)$, equal to $B_j(z)$, can be reformulated as follows:

$$\begin{aligned}
B_j(z) &= 1 - p_j(1 - \frac{\pi f_{rj}}{Q_j})z^{-1} + (1 - \frac{2\pi f_{rj}}{Q_j})z^{-2} \\
&= z^{-1}(z - 2\cos(2\pi f_{rj})(1 - \frac{\pi f_{rj}}{Q_j}) + (1 - \frac{2\pi f_{rj}}{Q_j})z^{-1}) \\
&= z^{-1}((z + z^{-1}) - \frac{2\pi f_{rj}}{Q_j}e^{2\pi f_{rj}} - 2\cos(2\pi f_{rj})(1 - \frac{\pi f_{rj}}{Q_j})) \\
&= z^{-1}(2\cos(2\pi f) - \frac{2\pi f_{rj}}{Q_j}e^{-j2\pi f} - 2\cos(2\pi f_{rj})(1 - \frac{\pi f_{rj}}{Q_j})) \\
&= z^{-1}(2(\cos(2\pi f) - \cos(2\pi f_{rj})) + (\cos(2\pi f_{rj}) - \cos(2\pi f))\frac{2\pi f_{rj}}{Q_j} + j\frac{2\pi f_{rj}}{Q_j}\sin(2\pi f)) \\
&= z^{-1}(2(\cos(2\pi f) - \cos(2\pi f_{rj}))(1 - \frac{\pi f_{rj}}{Q_j}) + j\frac{2\pi f_{rj}}{Q_j}\sin(2\pi f)) \\
&= z^{-1}(4\sin(\pi(f - f_{rc}))\sin(\pi(f + f_{rc}))(1 - \frac{\pi f_{rj}}{Q_j}) + j\frac{2\pi f_{rj}}{Q_j}\sin(2\pi f)).
\end{aligned} \tag{A.19}$$

Through the first order approximation around the modulator central frequency (resulting in: $\sin(\pi(f - f_{rc})) \approx (\pi(f - f_{rc}))$, it is possible to approximate $B_j(z)$ as follows:

$$B_j(z) \approx z^{-1}(4\pi(f - f_{rc})\sin(\pi(f + f_{rc}))(1 - \frac{\pi f_{rj}}{Q_j}) + j\frac{2\pi f_{rj}}{Q_j}\sin(2\pi f)). \tag{A.20}$$

Now, the modulus of the numerator of the $\mathrm{NTF}_j(z)$ can be expressed by:

$$|B_j(z)|^2 \approx 4\pi^2\sin^2(2\pi f_{rj})(4(f - f_{rj})^2 + (\frac{f_{rj}}{Q_j})^2). \tag{A.21}$$

The denominator of the $\mathrm{NTF}_j(z)$, equal to $c_j A_j(z)$, can be also reformulated as follows:

$$\begin{aligned}
c_j A_j(z) &= c_j(0.5p_j z^{-1} - z^{-2}) \\
&= c_j z^{-1}(0.5p_j - z^{-1}) \\
&= c_j e^{-j2\pi f_{rj}}(\cos(2\pi f_{rj}) - \cos(2\pi f) + j\sin(2\pi f)).
\end{aligned} \tag{A.22}$$

Then, the modulus of the denominator of the $\mathrm{NTF}_j(z)$ becomes as follows:

$$|c_j A_j(z)|^2 = c_j^2(|2\pi f_{rj}) - \cos(2\pi f)|^2 + |\sin(2\pi f)|^2) \quad \approx c_j^2 \left|\sin(2\pi f_{rj})\right|^2 . \tag{A.23}$$

As a result, the expression of the modulus of the $\mathrm{NTF}_j(z)$ is given by:

$$|\mathrm{NTF}_j(z)|^2 \approx \frac{4\pi^2}{c_j^2}(4(f - f_{rj})^2 + (\frac{f_{rj}}{Q_j})^2). \tag{A.24}$$

Finally, the modulus of the NTF of a 6^{th}-order MSCL employing band-pass resonators with a finite Q-factor is:

$$NTF(z) = \prod_{j=1}^{n} \frac{4\pi^2}{c_j^2}(4(f - f_{rj})^2 + (\frac{f_{rj}}{Q_j})^2). \tag{A.25}$$

Bibliography

[1] K. Grati, "Architecteure d'un Recepteur Radio Multistandard a Selection Numerique des Canaux", *Phd thesis*, L'ECOL PARIS-TELECOM, 2005. 1

[2] J. Mitola, "The Software Radio Architecture", *IEEE Communications Magazine*, vol. 33, no. 5, pp. 2638, 1995. 1

[3] J. Mitola, Z. Zvonar, "Software Radio Technologies", *IEEE Press*, 2001. 1

[4] L. Mitola, "Technical Challenges in the Globalization of Software Radio", *IEEE Communications Magazine*, vol. 37, no. 2, pp. 8489, 1999. 2

[5] W. Tuttlebee, "Software Defined Radio : Origins, Drivers and International Perspectives", *Book hand*, John Wiley and Sons, 2002. 2

[6] Y. Chiu, "High-Performance Pipeline A/D Converter Design in Deep-Submicron CMOS", *Phd thesis*, UNIVERSITY of CALIFORNIA, BERKELEY, 2004. 2

[7] S. KAWAHITO, "Techniques for Digitally Assisted Pipeline A/D Converters", *IEICE Transactions on Electronics*, pp. 829-836, 2008. 2

[8] G.C. Hadidi, K. Tso, V.S. Temes, "Fast Successive-Approximation A/D Converters", *IEEE Custom Integrated Circuits Conference*, pp. 6.1/1-6.1/4, May 1990. 2

[9] H. Neubauer, T. Desel, H. Hauer, "A successive Approximation A/D Converter with 16-bit 200 kS/s in0.6 μm CMOS Using Self Calibration and Low Power Techniques", *IEEEC Circuits and Systems*, vol. 2, pp. 859-862, July 2001. 2

[10] C.E. Onete, "Reconfigurable Flash A/D Converters", *IEEEC SOC Conference*, pp. 323-326, September 2008. 2

[11] Y. Geerts, M. Steyaert, "Flash A/D Specifications for Multi-bit ΣΔ A/D Converters", *IEEEC Circuits and Systems*, pp. 50-53, October 1999. 2

[12] J. van Valburg, R.J. van de Plassche, L. Philips Res, Endhoven; "An 8-b 650-MHz Folding ADC", *IEEE journal of Solid State Circuit*, pp. 1662-1666, vol. 27, December 1992. 2

[13] O. Carnu, A. Leuciuc, "Optimal Offset Averaging for Flash and Folding A/D Converters", *International Symposium on Circuits and Systems*, pp. 133-136, vol. 1, May 2004. 2

[14] A. Eshraghi, T. Fiez, "A Time-Interleaved Parallel ΣΔ A/D Converter", *IEEE Transaction Circuit and System .II*, vol. 50, pp. 118129, March 2003. 2

[15] I. Galton, H.T. Jensen, "Delta-sigma Modulator Based A/D Conversion without Oversampling", *IEEE Transaction Circuit and System .II*, vol. 42, no. 12, pp. 773784, December 1995. 2

[16] P. Aziz, H. Sorensen, J. Van der Spiegel, "Multi-band Sigma-Delta Modulation", *Electronics Letters*, pp. 760762, April 1993. 2, 35

[17] P. Aziz, H. Sorensen, J. Van der Spiegel, "Multi-band Sigma-Delta Analog to Digital Conversion", *IEEE ICASSP*, vol. 3, pp. 249252, April 1994. 2, 33

[18] P. Benabes, A. Beydoun, J. Oksman, "Extended Frequency-Band-Decomposition Sigma-Delta A/D Converter", *IEEE Analog Integrated Circuits and Signal Processing*, December 2008. 2

[19] A. Eshraghi, T. Fiez, "A Comparative Analysis of Parallel Delta-Sigma ADC Architectures", *IEEE Transaction Circuit and System .I*, vol. 51, pp. 450458, March 2004. 2, 35

[20] A. Beydoun, "SYSTME DE NUMRISATION HAUTES PERFORMANCES BASE DE MODULATEURS SIGMA-DELTA PASSE-BANDE", *Phd thesis*, L'Universite Paris XI. 3, 34, 35, 37, 43

[21] M. Ortmanns, F. Gerfers, "Continuous-Time Sigma-Delta A/D Conversion", *Bookhand*, Springer, 2006. 6, 19, 51

[22] W. R. Bennett, "Spectra of Quantized Signals", *Bell System Technology Journal*, vol. 27, pp.446-472, July 1948. 7

[23] B. Widrow, "A Study of Rough Amplitude Quantization by Means of Nyquist Sampling Theory", *IRE Transactions on Circuit Theory*, vol. 3, pp. 266-276, 1956. 7

[24] A.B. Sripad, D. L. Snyder, "A Necessary and Sufficient Condition for Quantization Errors to be Uniform and White", *IEEE Transactions on Acoustics, Speech and Signal Processing*, vol. 25, pp. 442-448, October 1977. 7

[25] N. Ahmed, T. Natarajan, "Discrete-Time Signals and Systems", *Book hand*, Prentice-Hall, Englewood Cliffs, NJ, 1983. 7

[26] J. C. Candy, O.J. Benjamin, "The Structure of Quantization Noise From Sigma-Delta Modulation", *IEEE Transactions on Communications*, vol. 29, no. 9, pp. 1316-1323, September 1981. 8

[27] V. Friedman, "Structure of the Limit Cycles in Sigma-Delta Modulation", *IEEE Transactions on Communications*, vol. 36, no. 8, pp. 972-979, August 1988. 8

[28] R. M. Gray, W. Chou, P. W. Wong, "Quantization Noise in Single-Loop Sigma-Delta Modulation with Sinusoidal Inputs", *IEEE Transaction On Communications*, vol. 37, no. 9, Pp. 956-967, September 1989. 8

[29] J. E. Iwersen, "Comments on the Structure of the Limit Cycles in Sigma-Delta Modulation", *IEEE Transactions on Communications*, vol. 38, no. 8, pp. 11-17, August 1990. 8

[30] M. Vidyasagar, "Nonlinear Systems Analysis", *Hand book*, Prentice-Hall, Englewood Cliffs, 1978. 8

[31] A. Gelbe, W. E. V. Velde, "Multiple-Input Describing Functions and Nonlinear Systems Design", *Hand book*, McGraw-Hill, 1968. 8

[32] D. P. Atherton, "Nonlinear Control Engineering", *Hand book*, Van Nostrand Reinhold, 1982. 8

[33] P. T. Maguire, Q. Huang, "Quantizer Gain in n^{th}-Order $\Sigma\Delta$ Modulator Linear Model : Its Determination Based on Constant Output Power Criterion", *Proceedings of lSCAS*, vol. 5, pp. 333-336, June 1994. 8

[34] L. Risbo, "Stability Predictions for High Order Sigma-Delta Modulators Based on Quasilinear Modeling", *IEEE International Symposium on Circuits and Systems*, pp. 361-364, April 1994. 8

[35] W. Chou, R. M. Gray, "Dithering and Its Effects on Sigma-Delta and Multistage Sigma-Delta Modulation", *IEEE Transaction on Information Theory*, vol. 37, no 3, pp. 500-513, May 1991. 9

[36] S. Jantzi, C. Ouslis, A. Sedra, "Transfer Function Design for AS Converters", *Proceedings of ISCAS*, vol. 5, pp. 433-436, June 1994. 9

[37] P. Benabes, M. Keramat, R.Kielbasa, "Synthesis and Analysis of Sigma-Delta Modulators Employing Continuous-Time Filters", *Analog Integrated Circuits and Signal Processing*, no 23, pp. 141-152, 2000. 9

[38] N. Scheinberg, D. Schilling, "Techniques for Correcting Transmission Error in Video Adaptive Delta-Modulation Channels", *IEEE Transaction Communications*, pp. 1064-1070, September 1977. 11

[39] H. Inose, Y. Yasuda, J. Marakami, "A Telemetering System by Code Modulation, Delta-Sigma Modulation", *IEEE Transaction Electronics and Telemetry*, pp. 204-209, September 1962. 12

[40] P. M. Aziz, H. V. Sorensen, J. Van Der Spieoel, "An Overview of Sigma-Delta Converters", *IEEE Signal Processing Magazine*, pp. 61-84, January 1996. 12

[41] P. Benabes, "Etude de Nouvelles Structures de Modulateurs Sigma-Delta Passe-Bande", *Phd thesis*, L'Universite Paris XI, 1994. 12, 165, 167

[42] D. Morche, "Conception de Codeurs Sigma-Delta en Technologie CMOS pour la Conversion Analogique-Numrique Haute Resolution", *Phd thesis*, L'Ecole INPOXI, 1994. 12

[43] S. Park, "Principles of Sigma-Delta Modulation for Analog-to-Digital Converters", *Digital Signal Processing Operation*, MOTOROLA, 1990. 12

[44] O. Shoaei, "Continuous-Time Delta-Sigma A/D Converters for High Speed Applications", *Phd thesis*, Carleton University, 1995. 15, 20, 51

[45] R. Schreier, W. M. Snelgrove, "Bandpass Sigma-Delta Modulation", *Electronics Letters*, vol. 25, pp. 1560-1561, November 1989. 15, 20

[46] L.A. Williams, B.A. Wooley, "Third-Order Cascaded Sigma-Delta Modulators", *IEEE Circuits and Systems*, vol. 38, issue 5, pp. 489-498, May 1991. 15, 20

[47] O. Shoaei, W. Snelgrove, "Design and Implementation of a Tunable 40-70 MHz Gm-C Bandpass Sigma-Delta Modulator ", *IEEE Transaction on Circuits and System II*, vol. 44, pp. 521-530, July 1997. 16, 31

[48] H. Tao, J. Khoury, "A 400-Ms/s Frequency Translating Bandpass Sigma-Delta Modulator", *IEEE Journal and Solid-State Circuits*, vol. 34, no. 12, pp. 1741-1752, December 1999. 16, 31

[49] W. Gao, W.M. Snelgrove, "A 950-MHz IF Second-Order Integrated LC Bandpass Delta-Sigma Modulator", *IEEE Journal and Solid-State Circuits*, vol. 33, no. 5, pp. 723-732, May 1998. 16, 31

[50] V.F. Dias, G. Palmisano, F. Maloberti, "Noise in Mixed Continuous-Time Switched-Capacitors Sigma-Delta Modulators", *IEE Proceeding-G*, vol. 139, no. 6, pp. 680-684, December 1985. 16

[51] J.A. Cherry, W.M. Snelgrove, "Clock Jitter and Quantizer Metastability in Continuous-Time Delta-Sigma Modulators", *IEEE Transactions on Circuits and Systems*, Vol. 46, No. 6, June 1999. 16

[52] A. Gosslau, A. Gottwald, "Optimization of a Sigma-Delta Modulator by the Use of a Slow ADC", *IEEE International Symposium on Circuits and Systems*, pp. 2317-2320, Jun. 1988. 17

[53] A. Gausslau, A.Gottwald, "Linearization of Sigma-Delta Modulator by a Proper Loop Delay", *International Symposium on Circuits Systems*, vol 1, pp. 364-367, 1990. 17

[54] A. YAHIA, "Contribution la Conception Automatis de Convertisseurs Analogique-Numrique Sigma-Delta Passe-Bande Rapides", *Phd thesis*, L'Universite Paris XI. xiii, 17, 19

[55] G. Fischer, A.J. Davis, "Alternative Topologies for Sigma-Delta Modulators- A Comparative Study", *IEEE Analog and Digital Signal Processing*, vol. 44, issue 10, pp. 789-797, October 1997. 20

[56] K. Uchimura, T. Hayashi, T. Kimura, A. Iwata, "Oversampling A/D and D/A Converters with Multi-Stage Noise Shaping Modulators", *IEEE Signal Processing*, pp. 1899-1905, December 1988. 20

[57] L.A. Williams, "Third Order Sigma Delta Modulators", *IEEE Circuits and Systems*, pp. 489-498, May 1991. 20

[58] P. Benabes, A. Gautier, D. Billet, "New Wide-band Sigma-Delta Convertor", *Electronic letters*, vol. 17, pp. 1575-1577, August 1993. 21

[59] N. Maghari, S. Kwon, G. C. Temes, and U. Moon, "Sturdy MASH Sigma-Delta Modulator", *Electronic letters*, pp. 1269-1270, vol. 42, October 2006. 21

[60] N. Maghari, Un-Ku Moon , "Multi-Loop Efficient Sturdy MASH Delta-Sigma Modulators", *IEEE International Symposium on Circuits and Systems*, pp. 1216-1219, May 2008. 21

[61] O. Shoaei, W.M. Snelgrove, "A Multi-Feedback Design for LC Bandpass Delta-Sigma Modulators", *Proceedings Inter Symposium on Circuits and Systems*, vol. 1, pp. 171-174, May 1995.

[62] A. Jayaraman, P. Asbeck, K. Nary, S. Beccue, "Bandpass Delta-Sigma Modulator with 800 MHz Center Frequency", *IEEE Anaheim conference on Gallium Arsenide Integrated Circuits*, pp. 95-98, October 1997. 22, 31

[63] J.A.E.P Van Engelen, R.J Van de Plassche, E. Stikvoort, A.G. Venes, "A Sixth-Order Continuous-Time Bandpass Sigma-Delta Modulator for Digital Radio IF", *IEEE Solid State Circuits*, vol. 34, issue 12, pp. 1753-1764, December 1999. 22, 31, 74

[64] Y. Xiaolong, T. Nianxiong, S. Signell, "On Low Power Design of Feedforward Continuous-Time Sigma Delta Modulators with Excess Loop Delay", *IEEE International Symposium on Circuits and Systems*, pp. 1882-1885, May 2008. 23

[65] S. Yan, E.S. Sinencio, "A Continuous-Time Sigma-Delta Modulator with 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth", *IEEE Journal of Solid State Circuits*, vol. 39, issue 1, pp. 75-86, January 2004. 23

[66] G. Mitteregger, C. Ebner, S. Mechnig, T.Blon, C. Holuigue, E. Romani, A. Melodia, V. Melini, "A 14b 20mV 640MHz CMOS CT Sigma Delta ADC with 20MHz Signal Band Width and 12b ENOB ", *IEEE International conference of Solid state Circuits*, pp. 131-140, vol. 1, February 2006. 23

[67] S. Paton, A. D. Giandomenico, L. Hernandez, A. Wiesbauer, P. Potscher, M. Clara, "A 70-mv 300 MHz CMOS Continuous-Time Sigma-Delta ADC with 15-MHz Band Width and 11-bits of resolution", *IEEE Journal of Solid State Circuits*, pp. 1056-1062, vol. 39, July 2004. 23

[68] Z. Li, T. S. Fiez, "A 14 bit 5 MS/s Continuous-Time Delta-Sigma A/D Modulator", *IEEE International Symposium on VLSI Circuits*, pp. 164-165, vol. 31, June 2006. 23

[69] C. Wolf, L. R. Carely, "Modeling the Quantizer in High-Order Delta-Sigma Modulators ", *IEEE ISCAS*, pp. 2335-2339, June 1998. 25

[70] R. W. Adams, "Theory and Practical Implementation of a Fifth-Order Sigma-Delta A/D Converter", *J. Audio Engineering Society*, vol. 39, pp. 515-528, July 1991. 25

[71] S. H. Ardalan, J. J. Paulos, "An Analysis of Non-Linear Behavior in Delta-Sigma Modulators", *IEEE Circuits and Systems*, vol. 34, no. 6, pp. 593-603, June 1987. 25, 39

[72] R. Schreier, "An Emprical Study of High-Order Single-Bit Delta-Sigma Modulator", *IEEE Circuits and Systems*, vol. 40, no. 8, pp. 461-466 August 1993. 25, 27

[73] L. Risbo, "Sigma-Delta Modulators, Stability Analysis and Optimization", *Phd thesis*, Technical University of Denmark, 1994. 25

[74] L. Risbo, "FPGA Based 32-Times Oversampling 8th-Order Sigma-Delta Audio DAC", *AES Convention*, February 1994. 25

[75] G. Thaler, M. Pastel, "Analysis and Design of nonlinear feedback control systems", *Hand book*, McGraw-Hill, 1992. 26

[76] T. Ritoniemi, T. Karema, H. Tenhunen, "Design of Stable High-Order 1-Bit Sigma-Delta Modulators", *IEEE ISCAS*, pp. 3267-3270, May 1990. 26

[77] W. Lee "A Novel Higher Order Interpolative Modulator Topology for High Resolution Oversampling A/D Converters", *Master thesis*, Massachusetts Institute of Technology, 1987. 27

[78] K.C.H Chao, S. Nadeem, W.L. Lee, C.G. Sodini, "A Higher Order Topology for Interpolative Modulators for Oversampling A/D Conversion", *IEEE Circuits and Systems*, vol. 37, pp. 309-318, March 1990. 27

[79] R. Schreier, G.C. Temes "Understanding Delta-Sigma Data Conversion", *Book hand* John Wiley and Sons 2005. 27

[80] I.D. Landau, F. Rolland, C. Cyrot, A. Voda, "Digital Robust Control, The Combined Pole Placement/ Sensitivity Shaping Method", *Report*, Laboratoire d'Automatique de Grenoble, 1993 28

[81] C. Banyasz, L. Keviczky, "A New Gap Metric for Robustness Measure and Regulator Design", *Control and Automation*, June 2001. 28

[82] W. L. Lee, C. G. Sodini, "A Topology for Higher-order Interpolative Coders", *IEEE International Symposium on Circuits and Systems*, pp.459-462, May 1987. 30

[83] H. A. Spang, P. M. Schultheiss, "Reduction of Quantizing Noise by Use of Feedback", *IRE Transaction Communication Systems*, vol. CS-10, pp. 373-380, December 1962. 31

[84] H. Inose, Y. Yasuda, "A Unity Bit Coding Method by Negative Feedback", *IEEE*, vol. 51, pp. 1524-1535, November 1963. 31

[85] J.C. Candy, " Use of Limit Cycle Oscillations to Obtain Robust Analog-to-Digital Converters", *IEEE Transaction On Communications*, vol. COM-22, pp. 298-305, March 1974. 31

[86] J.C. Candy, W.E. Ninke, B.A. Wooley, " Per-Channel A/D Converter Having 15-Segment n-255 Companding", *IEEE Transaction On Communications*, vol. COM-24, pp. 33-42, January 1976. 31

[87] R.J. Van De Plassche, "A Sigma-Delta Modulator as an A/D Converte", *IEEE Transaction On Circuits and Systems*, vol. CAS-25, pp. 510-514, July 1978. 31

[88] T. Misawa, J.E. Iwersen, L.J. Loporcaro, J.G. Ruch, "Single-Chip Per Channel Codee with Filters Utilizing Sigma-Delta Modulation", *IEEE Journal of Solid-State Circuits*, vol.SC-16, pp. 333-341, August 1981. 31

[89] *Sirrus logic, http//:www.sirrus.com* 31

[90] B. Del Signore, D.A. Kerth, N.S. Sooch, E.J. Swanson, "A Monolithic 20b Delta-Sigma A/D Converter", *IEEE Solid-State Circuits*, vol. SC-25, pp.1311-1316, December 1990. 31

[91] M. Sarhang-Nejad, G. Ternes, "A High-Resolution Multibit Sigma-Delta ADC with Digital Correction and Relaxed Amplifier Requirements", *IEEE Solid-State Circuits*, pp. 648-660, June 1993. 31

[92] L.A. Williams, B.A. Wooley, "A Third-Order Sigma-Delta Modulator with Extended Dynamnic Range", *IEEE Solid-State Circuits*, vol. 29, no. 3, pp. 193-202, March 1994. 31

[93] J.A. Cherry, W.M.W. Gao, "On the Design of a Fourth-Order Continuous-Time LC Delta-Sigma Modulator for UHF A/D Conversion", *IEEE Circuits and Systems*, vol. 47(6) pp. 518530, 2000. 31

[94] W. Gao, A. Cherry, W.M. Snelgrove, "A 4 GHz Fourth-Order SiGe HBT Band Pass Delta-Sigma Modulator", *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 174175, June 1998. 31

[95] A.E. Cosand, J.F. Jensen, " IF-Sampling Fourth-Order Band-Pass Delta-Sigma for Digital Receiver Applications", *IEEE solid-state circuit*, vol. 39(10) pp. 16331639, 2004. 31

[96] S. Benabid, " Contribution a la Conception dun Convertisseur Sigma-Delta Passe-Bande a Temps Continu dans une Technologie Standard CMOS", *Phd thesis*, L'UNIVERSITE PARIS XI, 2005. 31, 56

[97] R. Maurino, P. Mole, " A 200-MHz IF 11-bit Fourth-Order Band-Pass Sigma-Delta ADC in SiGe", *IEEE Solid-State Circuits*, vol. 35, no. 7, pp. 959967, July 2000. 31

[98] C. H. Kuo, S. I. Liu, " A 1-V 10.7-MHz Fourth-Order Band-Pass Sigma-Delta Modulators Using Two Switched OpAmps", *IEEE Solid-State Circuits*, vol. 39, no. 11, pp. 20412045, November 2004. 31

[99] X. Wang, Y.P Xu, Z. Wang, S. Liw, " A Band-Pass Sigma-Delta Modulator Employing Micro-Mechanical Resonator", *IEEE Circuits and Systems*, vol. 1, pp. 1041, May 2003. 32

[100] R. Yu, Y.P. Xu, " Band-pass Sigma-Delta Modulator Employing SAW Resonator as Loop Filter", *IEEE Transactions on Circuits and Systems*, vol. 54, no. 4, April 2007. 32

[101] P. Vaidyanathan, "Multi-Rate Systems and Filter Banks", *Hand book*, rentice-Hall, Inc. Upper Saddle River, NJ, USA, 1993. 33

[102] P. Benabes, A. Beydoun, R. Kielbasa, "Bandpass Wide-Band ADC Architecture Using Parallel Delta-Sigma Modulators", *14th European Signal Processing Conference*, 2006. 35

[103] P. Benabes, A.Gauthier, R. Kielbasa, "A Multistage Closed-Loop Sigma-Delta Modulator (MSCL)", *Analog integrated circuits and signal processing*, 11, 195-204, 1996. 36

[104] S. Benabid, E. Najafi-Aghdam, P. Benabes, S. Guessab and R.Kielbasa, "CMOS Design of a Multibit Band-pass Continuous-Time Sigma-Delta Modulator Running

at 1.2 GHz“, *IEEE International Caracas Conference on Devices, Circuits and Systems*, pp. 5155, November 2004. 39

[105] S. Norsworthy, R. Schreier, G. Temes, “Delta Sigma Data Converters: Theory, Design, and Simulation“, *IEEE Press*, 1996. 43

[106] J. Maeyer, J. Raman, P. Rombouts and L. Weyten, “Controlled behaviour of STF in CT Delta-Sigma Modulators“, *Electronics letters* , vol. 41, August 2005. 52

[107] M. Ranjbar, A. Mehrabi and O. Oliaei “Continuous-Time Feed-forward Delta-Sigma Modulators with Robust Signal Transfer Function“, *IEEE Circuits and Systems* , vol. 18, issue 21, pp. 1878-1881, May 2008. 52

[108] S. Pipilos, Y.P. Tsividis, J. Fenk, Y. Papananos, “A Si 1.8 GHz RLC Filter with Tunable Center Frequency and Quality Factor“, *IEEE Journal of solid state circuits*, 31, October 96. 56

[109] WB Kuhn, FW Stephenson, A. Elshabini-Riad, “Dynamic Range of High-Q OTA-C and Enhanced-Q LC RF Bandpass Filters“, *Circuits and Systems*, vol. 2, 1994. 56

[110] C. Toumazou, D. G. Haigh, “Integrated Microwave Continuous-Time Active Filter Using Fully Tunable GaAs Transconductors“, *IEEE International Symposium on Circuits and Systems*, 3 :17651768, June 91. 57

[111] U. Yodprasit, J. Ngarmnil, “Q-Enhancing Technique for RF CMOS Active Inductor“, *IEEE International Symposium on Circuits and Systems* , 5 :589592, Mai 2000. 57

[112] E. Avignon “Contribution Conception d’un Modulateur Sigma-Delta Passe-Bande Temps Continu pour la Conversion Direct de Signaux Radiofrequences“, *Phd thesis*, L’Universite Paris XI. 57

[113] M. Banu, Y. Tsividis, “Fully Integrated Active RC Filters in MOS Technology“, *IEEE Journal of Solid State Circuit*, vol. 18, pp. 644-651, December 83. 57

[114] M. Banu, Y. Tsividis, “Continuous Time MOSFET-C Filters in VLSI“, *IEEE Journal of Solid State Circuit*, vol. 21, pp. 15-30, February 86. 57

[115] W.B. Kuhn, W. Stephenson, A.E. Riad, "A 200 MHz CMOS Q-Enhanced LC Bandpass Filter", *IEEE Journal of Solid State Circuit*, 31, August 96. 57

[116] Y.P. Tsividis, "Integrated Continuous-Time Filter Design - An Overview", *IEEE Journal of solid state circuits* , 29(3), Mars 94. 57

[117] F.D. Bannon, J.R. Clark, C.T. Nguyen, "High-Q HF Microelectromechanical Filters", *IEEE Solid-State Circuits*, vol. 35, no. 4, April 2000. 58

[118] V. Kaajakari, T. Mattila, A. Oja, Kiihamki, H. Sepp, "Square-Extensional Mode Single-Crystal Silicon Micromechanical Resonator for Low Phase Noise Oscillator Applications", *IEEE Electron Device Letters*, vol. 25, no. 4, pp. 173-175, April 2004. 58

[119] S.-S. Li , Y.-W. Lin, Y. Xie, Z. Ren, C.T Nguyen, "Micromechanical Hollow-Disk Ring Resonators", *IEEE International conference on Micro Electro Mechanical Systems*, pp. 821-824, 2004. 58

[120] S. Pourkamali, F. Ayazi, "High Frequency Capacitive Micromechanical Resonators with Reduced Motional Resistance Using the HARPSS Technology", *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 147-150, 8-10 September 2004. 58

[121] T. Mattila, A. Oja, H. Seppa, O. Jaakkola, Kiihamaki, H. Kattelus, M. Koskenvuori, P. Rantakari, I. Tittonen, "Micromechanical Bulk Acoustic Wave Resonator", *IEEE Ultrasonics Symposium*, vol. 1, pp. 945-948, 8-11 October 2002. 58

[122] J. Wang, J. E. Butler, T. Feygelson, and C. T.-C. Nguyen, "1.51-GHz polydiamond micromechanical disk resonator with impedancemismatched isolating support", *Technical Digest, IEEE International MicroElectro Mechanical Systems Conference*, pp. 641-644, January 2004. 58

[123] J. Wang, Z. Ren, and C. T.-C. Nguyen, "1.156-GHz self-aligned vibrating micromechanical disk resonator", *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 51, no. 12, pp. 1607-1628, December 2004. 58

[124] M. z. Atashbar, B. 1. Bazuin, and S. Krishnamurthy, "Design and simulation of SAW sensors for wireless sensing", *IEEE sensors* 2003, pp. 584-589, 2003. 59

[125] M. Solal, J. Gratier, T. Kook, "A SAW resonator with two-dimensional reflectors", *IEEE International Symposium on Frequency Control*, pp. 226-231, April 2009. 59

[126] S. A. Mousavi, M. N. Hamidon, R. Sidek, M. Rahimi, "Design and simulation of one-port SAW resonator for wireless and high temperature application", *IEEE International Conference on Semiconductor Electronics*, pp. 18-22, November 2008. 60

[127] http://www.golledge.com/docs/products/saws.htm?g8b, 2007. 60

[128] R. Aigner, "High performance RF-filters suitable for above IC integration: film bulk-acoustic- resonators (FBAR) on silicon", *Proceedings of the IEEE Conference Custom Integrated Circuits*, pp. 141-146, September 2003. 60

[129] A.P.S. Khanna, Ed. Gane, T. Chong, Ko. Herb, P. Ruby, D. John, "A Film Bulk Acoustic Resonator (FBAR) L Band Low Noise Oscillator for Digital Communications", *European Microwave Conference*, pp. 1-3, October 2002. 60

[130] H.P. Loebl, C. Metzmacher, D.N. Peligrad, R. Mauczok, M. Klee, W. Brand, R.F. Milsorn, P. Lok, R. Van Straten, A. Tuinhout, J.W. Lobeek, "Solidly mounted bulk acoustic wave filters for the GHz frequency range", *IEEE Ultrasonics Symposium*, pp. 919-923, October 2002. 60, 61

[131] M. Desvergne, "Etude des Rsonateurs MEMS Ondes de Lamb Application au Filtrage en Frquence Intermdiaire dans les Rcepteurs de Radiotlcommunication", *Phd thesis*, L'Universite Bordeaux 1. xxi, 61, 63, 64

[132] V.M. Yantchev, I. Katardjiev, "Propagation characteristics of the fundamental symmetric Lamb wave in thin aluminum nitride membranes with infinite gratings", *Journal of Applied Physics*, vol.98, Issue 8, 2005. 61

[133] V.M. Yantchev, I. Katardjiev, "Micromachined thin film plate acoustic resonators utilizing the lowest order symmetric Lamb wave mode", *IEEE Transaction on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 54, Issue 1, pp. 87-95, January 2007. 61

[134] A.Volatier, G. Caruyer, D. Pellissier, P. Ancey, E. Defa, B. Dubus, "UHF/VHF resonators using Lamb Waves co-integrated with Bulk Acoustic Wave Resonators", *IEEE Ultrasonics Symposium*, vol.2, pp. 902-905, 18-21 September 2005. 61, 62, 67

[135] R.S. Naik, J.J. Lutsky, R. Reif, C.G. Sodini, "Electromechanical Coupling Constant Extraction of Thin-Film Piezoelectric Materials Using a Bulk Acoustic Wave Resonator", *IEEE Ultrasonics Symposium*, vol.2, pp. 902-905, 18-21 September 2005. 62

[136] "ATILA Users Manual version 5.2.3", *Laboratoire acoustique, Institut Superieur Electronique du Nord*, 2003. 63

[137] J. Bjrstrm, I. Katardjiev, V. Yantchev, "Lateral-Field-Excited Thin-Film Lamb Wave Resonator", *Applied Physics Letters*, vol. 86, Issue 15, id. 154103, 2005. 67

[138] V.M. Yantchev, I. Katardjiev, "Micromachined Thin Film Plate Acoustic Resonators Utilizing the Lowest Order Symmetric Lamb Wave Mode", *IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control*, vol. 54, Issue 1, pp. 87-95, Jan. 2007. 67

[139] S. Hamad, R. Abdolvand, G.K. Ho, G. Piazza, F. Ayazi, "High Frequency Micromachined Piezo-on-Silicon Block Resonators", *IEEE International Electron Devices Meeting*, 8-10 Dec. 2003. 67

[140] G. Piazza, P.J. Stephanou, A.P. Pisano, "Aluminum Nitride Contour-Mode Vibrating RF MEMS", *IEEE MTT-S Inter. Microwave Symposium Digest*, pp. 664-667, 2006. 67

[141] . Jayaraman, P. Asbeck, K. Nary and S. Beccue, "Bandpass Delta-Sigma Modulator with 800 MHz Center Frequency", *IEEE Anaheim conference on Gallium Arsenide Integrated Circuits*, pp. 95-98, October 1997. 74

[142] M. Keller, A. Buhmann, M. Ortmanns and Y. Manoli, "A Comparative Study on Excess Loop Delay Compensation Techniques for Continuous-Time Sigma-Delta Modulators", *IEEE Transaction on Circuits and Systems I*, pp. 3480-3487, December 2008. 74

[143] E. Najafi Aghdam, "NOUVELLES TECHNIQUES D'APPARIEMENT DYNAMIQUE DANS UN CNA MULTIBIT POUR LES CONVERTISSEURS SIGMA-DELTA", *Phd thesis*, L'Universite Paris XI, June 2006. 74

[144] S. Norsworthy, R. Schreier, and G. Temes, "Delta-sigma data converters, Theory, design and simulation", *IEEE Press*, 1997. 74

[145] B. Leung and S. Sutarja, "Multi-bit A/D converter incorporating a novel class of dynamic element matching techniques", *IEEE Transaction on Circuit and Systems II*, vol. CASII-39, pp. 35-51, January 1992. 74

[146] R. Schreier and G. Temes, "Understanding Delta-sigma data converters", *IEEE Press*, 2005. 74

[147] F. Chen and B. Leung, "A high resolution multibit sigma-delta modulator with individual level averaging", *IEEE Journal of Solid-State Circuits*, vol. SC-30, pp. 453-60, April 1995. 74

[148] F. Maloberti, "Analog Design for CMOS VLSI Systems", *Bookhand*, Kluwer, 2001. 121

[149] H. Fiedler, "A 5-bit Building-Block for 20 MHz A/D Converters", *IEEE Journal on Solid-State Circuits*, vol. SC-16, no. 3, pp. 151-155, September 1981. 121

[150] K. Yoon, S. Park, W. Kim, "A 6b 500MSample/s CMOS Flash ADC with a Background Interpolated Auto-Zeroing Technique", *IEEE Solid-State Circuits Conference*, pp. 326-327, February 1999. 121

[151] S. Tsukamoto, W. G. Schoeld, T. Endo, "A CMOS 6-b 400-Msamples/s ADC with Error Correction", *IEEE Journal of Solid-State Circuits*, vol. 33, no.12, pp. 1939-1947, December 1998. 121

[152] J. Ho, H.C. Luong, "A 3-V , 1.47-mW, 120-MHz Comparator for Use in a Pipeline ADC", *Proc. of IEEE Asia Pacific Conference on Circuits and System*, pp. 413-416, November 1996. 121

[153] C. A. Tugui "High Performance Converters Bank Using Parallel BandPass Sigma-Delta Modulators: Transistor Level Simulation of a Sigma-Delta Modulator Using Lamb Waves", *Internship report*, Ecol Supelec, July 2009. 158

[154] "Versanum project report", *French research agency*,ANR-05.RNRT-010-01. 158, 163

Declaration

I herewith declare that I have produced this paper without the prohibited assistance of third parties and without making use of aids other than those specified; notions taken over directly or indirectly from other sources have been identified as such. This paper has not previously been presented in identical or similar form to any other Fench or foreign examination board.

The thesis work was conducted from 2006 to 2009 under the supervision of Phillipe Benabes at Department of Signals processing and Electronic Systems (SSE), SUPELEC.

Paris, France

Publications

- M. Javidan, P. Benabes,
  A new method to synthesize and optimize band-pass delta-sigma modulators,
  6^{th} International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference (NEWCAS-TAISA),
  page(s): 197-200, June 2008.

- M. Javidan, P. Benabes,
  Band-pass continuous-time delta-sigma modulators employing LWR resonators,
  15^{th} IEEE International Conference on Electronics, Circuits and Systems (ICECS),
  page(s): 1119-1122, August 2008.

- P. Benabes, A. Beydoun, M. Javidan,
  Frequency-band-decomposition converters using continuous-time sigma-delta A/D modulators,
  7^{th} International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference (NEWCAS-TAISA),
  2009.

- M. Javidan, P. Benabes,
  A 6^{th}-order single-stage feed-forward band-pass continuous-time sigma-delta modulator,
  IEEE Transaction on Circuits and Systems-I:Analog and Digital Signal Processing,

Submitted.

- M. Javidan, P. Benabes,
  Design of electronic control circuit of piezo-electric resonators for $\Sigma\Delta$ modulator loop in AMS Bi-CMOS $0.35\mu\ m$,
  IEEE International Symposium on Circuits and Systems (ISCAS),
  Submitted.